



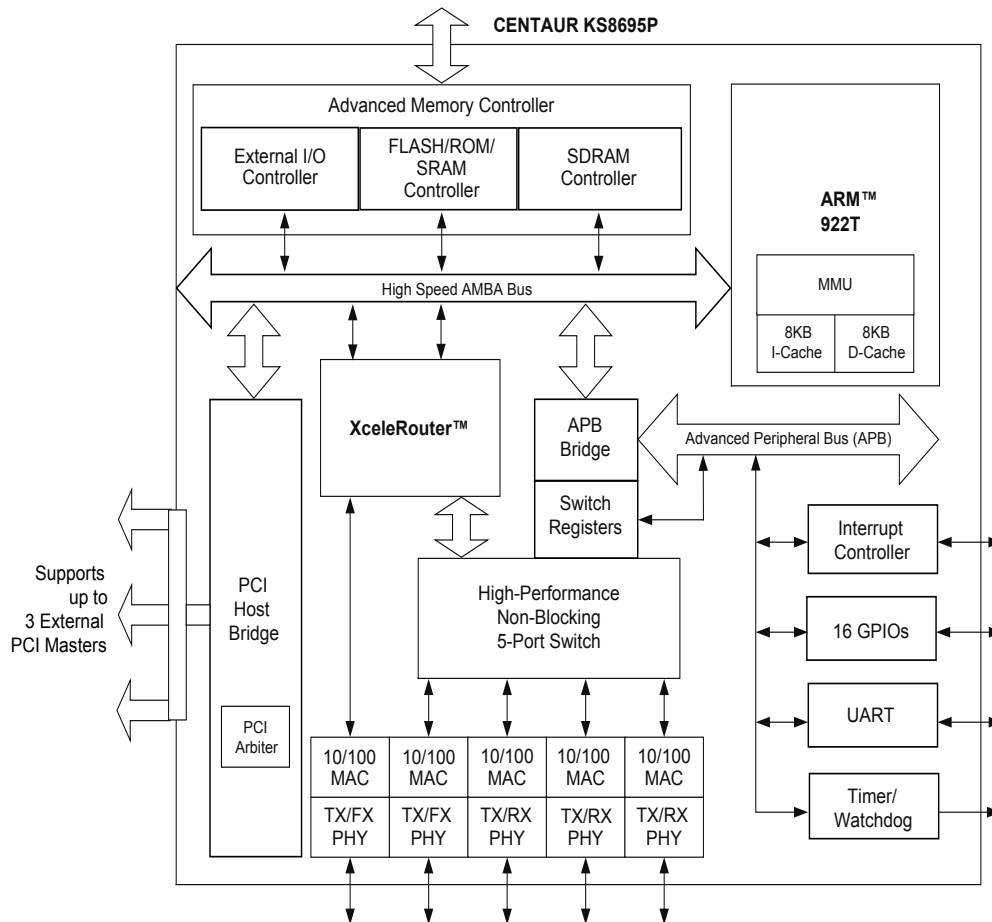
General Description

The CENTAUR KS8695P, Multi-Port PCI Gateway Solution, delivers a new level of networking integration, performance, and overall BOM cost savings, enabling original equipment manufacturers (OEMs) to provide customers with feature-rich, low-cost solutions for the residential gateway and small office environment.

- Integration of a PCI arbiter supporting three external masters.
 - Allows incorporation of a variety of productivity enhancing system interfaces, including the expanding 802.11 a/g/b wireless LAN.
- High-performance ARM™ CPU (ARM9) with 8KB I-cache, 8KB D-cache, and a memory management unit (MMU) for Linux and WinCE® support.

- XceleRouter™ technology to accelerate packet processing.
- Proven wire-speed switching technology that includes 802.1Q tag-based VLAN and quality of service (QoS) support.
- Five patented mixed-signal, low-powered Fast Ethernet transceivers with corresponding media access control (MAC) units.
- Advanced memory interface with programmable 8/16/32-bit data and 22-bit address bus with up to 64MB of total memory space for Flash, ROM, SRAM, SDRAM, and external peripherals.

Functional Diagram



XceleRouter is a trademark of Micrel, Inc. AMD is a registered trademark of Advanced Micro Devices, Inc. ARM is a trademark of Advanced RISC Machines Ltd. Intel is a registered trademark of Intel Corporation. WinCE is a registered trademark of Microsoft Corporation.

Features

The CENTAUR KS8695P featuring XceleRouter technology is a single-chip, multi-port PCI "gateway-on-a-chip" with all the key components integrated for a high-performance and low-cost broadband gateway

- **ARM9 High-Performance CPU Core**
 - ARM9 core at 166MHz
 - 8KB I-cache and 8KB D-cache
 - Memory management unit (MMU) for Linux and WinCE
 - 32-bit ARM and 16-bit thumb instruction sets for smaller memory footprints
- **33MHz 32-Bit PCI Interface**
 - Version PCI 2.1
 - Supports bus mastership or guest-mode
 - Supports normal and memory-mapped I/O
 - Support for miniPCI and cardbus peripherals
- **Integrated Ethernet Transceivers and Switch Engine**
 - Five 10/100 Ethernet transceivers and five MACs (1P for WAN interface, 4P for LAN switching)
 - 100BASE-FX mode option on the WAN port and one LAN port
 - Automatic MDI/MDI-X crossover on all ports
 - Wire-speed, non-blocking switch
 - 802.1Q tag-based VLAN (16 VLANs, full range VID)
 - Port-based VLAN
 - QoS/CoS packet prioritization support: per port, 802.1p, and DiffServ-based
 - 64KB on-chip frame buffer SRAM
 - VLAN ID and 802.1P tag/untag option per port
 - 802.1D Spanning Tree Protocol support
 - Programmable rate-limiting per port: 0Mbps to 100Mbps, ingress and egress, rate options for high and low priority
 - Extensive MIB counter management support
 - IGMP snooping for multicast packet filtering
 - Dedicated 1K entry look-up engine
 - Port mirroring/monitoring/sniffing
 - Broadcast and multicast storm protection with % control global and per port basis
 - Full- and half-duplex flow control
- **XceleRouter Technology**
 - TCP/UDP/IP packet header checksum generation to offload CPU tasks
 - IPv4 packet filtering on checksum errors
 - Automatic error packet discard
 - DMA engine with burst-mode support for efficient WAN/LAN data transfers
 - FIFOs for back-to-back packet transfers

- **Memory and External I/O Interfaces**
 - 8/16/32-bit wide shared data path for Flash, ROM, SRAM, SDRAM, and external I/O
 - Total memory space up to 64MB
 - Intel®/AMD®-type Flash support
- **Peripheral Support**
 - 8/16/32-bit external I/O interface supporting PCMCIA or generic CPU/DSP host I/F
 - Sixteen general purpose input/output (GPIO)
 - Two 32-bit timer counters (one watchdog)
 - Interrupt controller
- **System Design**
 - Up to 166MHz CPU and 125MHz bus speed
 - 289 PBGA package (19mm x 19mm) saving board real estate
 - Two power supplies: 1.8V core and Ethernet RX supply, 3.3V I/O and Ethernet TX supply
 - Built-in LED controls
- **Debugging**
 - ARM9 JTAG debug interface
 - UART for console port or modem back-up
- **Power Management**
 - CPU and system clock speed step-down options
 - Low-power Ethernet transceivers
 - Per port power-down and Ethernet transmit disable
- **Reference Hardware and Software Evaluation Kit**
 - Hardware evaluation board (passes class B EMI)
 - Board support package including firmware source codes, Linux kernel, and software stacks
 - Complete hardware and software reference designs available

Applications

- Multi-port wireless VoIP gateway
- Wireless mesh network node
- RG + combo 802.11 a/b/g/n access point
- Multimedia gateway
- Digital audio access point
- Network storage element
- Multi-port broadband gateway
- Multi-port firewall and VPN appliances
- Combination wireless and wireline gateway
- Fiber-to-the-home managed CPE

Ordering Information

| Part Number | | | Temperature Range | Package |
|-------------|----------|----------------|-------------------|--------------|
| Industrial | Standard | Pb (lead)-Free | | |
| — | KS8695P | KSZ8695P | 0°C to +70°C | 289-Pin PBGA |
| KS8695PI | — | — | -40°C to +85°C | 289-Pin PBGA |

Revision History

| Revision | Date | Summary of Changes |
|-----------------|-------------|--|
| 0.9 | 05/13/03 | Created. |
| 0.91 | 06/04/03 | Corrected WRSTPLS sets WRSTO to active low when '1', and active high when '0'. |
| 0.92 | 06/10/03 | Changed pin A1 to GND. Changed pin E3, H7, J7, K7, L7 to AGND. Changed Figure 5 WRSTPLS to pull up. |
| 0.93 | 07/11/03 | Removed PCI 2.2 compliance. Removed TM from Centaur. Added LANFXSD1 signal description. |
| 0.94 | 07/17/03 | Updated DC Electrical Characteristics. |
| 0.95 | 08/11/03 | Added addressing description to memory controller and address pin description Table 11. Changed PRSTN to input in Table 10. |
| 1.0 | 09/2/03 | Changed Figure 1. Removed old register address tables and replaced with Figure 11. Added Memory Interface examples, Figures 7,8, and 9. Added memory interface description, section 2.5. |
| 1.1 | 09/29/03 | Changed Figure 2. |
| 1.2 | 08/04/04 | Transferred to Micrel format and updated System Clock. |
| 1.3 | 1/27/05 | Added recommended reset circuit. |
| 1.4 | 8/18/05 | Added wireless applications. Added Pb-Free and industrial specification. Edits to Pin Description Table. |

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System Level Applications

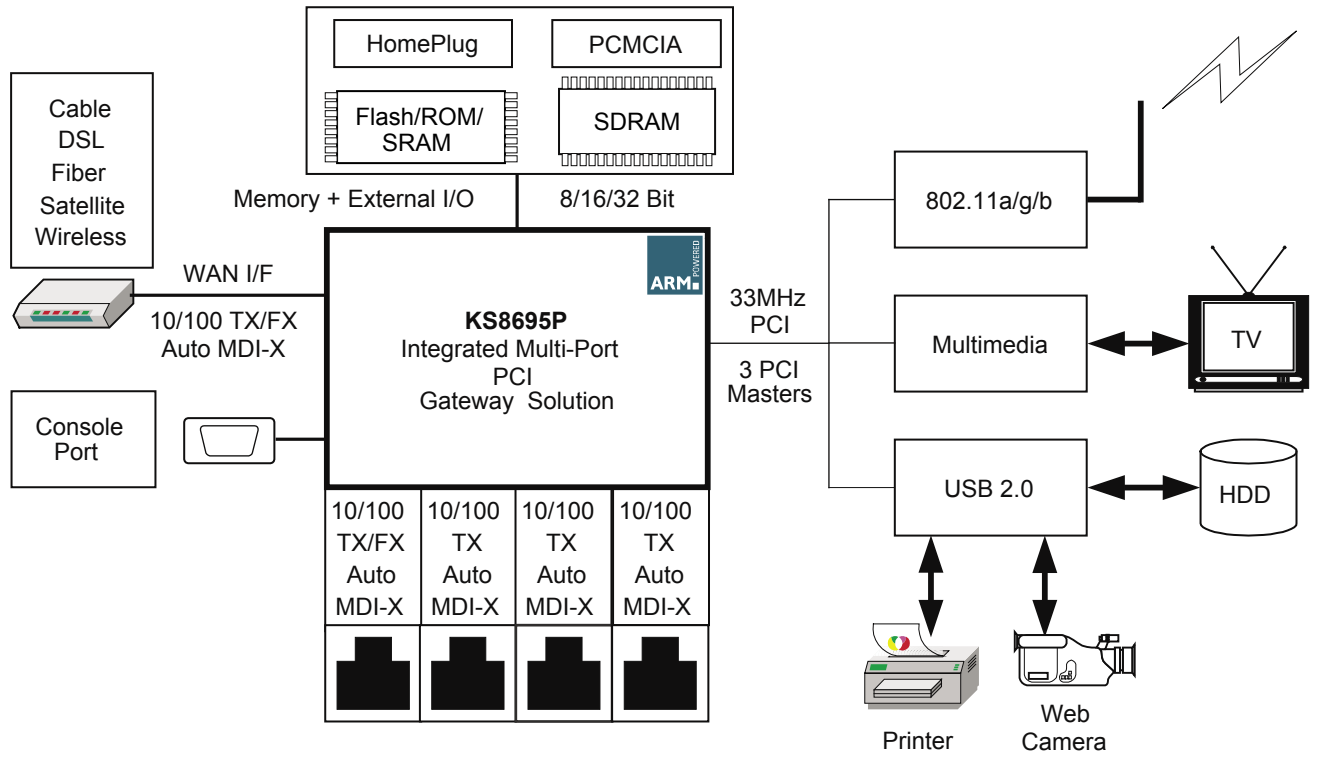


Figure 1. KS8695P PCI Gateway System Options

Pin Description**Signal List Alphabetized by Name**

| Pin Number | Pin Name | Type ⁽¹⁾ | Pin Function |
|------------|------------|---------------------|---|
| U4 | ADDR0 | O | Address Bit. |
| T4 | ADDR1 | O | Address Bit. |
| R3 | ADDR10 | O | Address Bit. |
| P1 | ADDR11 | O | Address Bit. |
| P2 | ADDR12 | O | Address Bit. |
| N1 | ADDR13 | O | Address Bit. |
| N2 | ADDR14 | O | Address Bit. |
| N3 | ADDR15 | O | Address Bit. |
| N4 | ADDR16 | O | Address Bit. |
| M1 | ADDR17 | O | Address Bit. |
| M2 | ADDR18 | O | Address Bit. |
| M3 | ADDR19 | O | Address Bit. |
| U3 | ADDR2 | O | Address Bit |
| P3 | ADDR20/BA0 | O | Address Bit/Bank Address Bit 0 for SDRAM Interface. |
| P4 | ADDR2/BA1 | O | Address Bit/Bank Address Bit 1 for SDRAM Interface. |
| T3 | ADDR3 | O | Address Bit. |
| U2 | ADDR4 | O | Address Bit. |
| U1 | ADDR5 | O | Address Bit. |
| T1 | ADDR6 | O | Address Bit. |
| T2 | ADDR7 | O | Address Bit. |
| R1 | ADDR8 | O | Address Bit. |
| R2 | ADDR9 | O | Address Bit. |
| E3 | AGND | Gnd | Analog Signal Ground. |
| H7 | AGND | Gnd | Analog Signal Ground. |
| J7 | AGND | Gnd | Analog Signal Ground. |
| K7 | AGND | Gnd | Analog Signal Ground. |
| L7 | AGND | Gnd | Analog Signal Ground. |
| D14 | CBEN0 | I/O | PCI Commands and Byte Enable 0. Active Low. |
| A11 | CBEN1 | I/O | PCI Commands and Byte Enable 1. Active Low. |
| B9 | CBEN2 | I/O | PCI Commands and Byte Enable 2. Active Low. |
| A6 | CBEN3 | I/O | PCI Commands and Byte Enable 3. Active Low. |
| B10 | CLKRUNN | I/O | Cardbus Clock Run Request Signal. Active Low. |
| U15 | DATA0 | I/O | External Data Bit. |
| T15 | DATA1 | I/O | External Data Bit. |
| U12 | DATA10 | I/O | External Data Bit. |
| T12 | DATA11 | I/O | External Data Bit. |

Note:

1. Gnd = Ground.

O = Output.

I/O = Bidirectional.

| Pin Number | Pin Name | Type ⁽¹⁾ | Pin Function |
|------------|---------------------|---------------------|--|
| R12 | DATA12 | I/O | External Data Bit. |
| P12 | DATA13 | I/O | External Data Bit. |
| U11 | DATA14 | I/O | External Data Bit. |
| T11 | DATA15 | I/O | External Data Bit. |
| R11 | DATA16 | I/O | External Data Bit. |
| P11 | DATA17 | I/O | External Data Bit. |
| U10 | DATA18 | I/O | External Data Bit. |
| T10 | DATA19 | I/O | External Data Bit. |
| U14 | DATA2 | I/O | External Data Bit. |
| R10 | DATA20 | I/O | External Data Bit. |
| P10 | DATA21 | I/O | External Data Bit. |
| U9 | DATA22 | I/O | External Data Bit. |
| T9 | DATA23 | I/O | External Data Bit. |
| R9 | DATA24 | I/O | External Data Bit. |
| P9 | DATA25 | I/O | External Data Bit. |
| U8 | DATA26 | I/O | External Data Bit. |
| T8 | DATA27 | I/O | External Data Bit. |
| R8 | DATA28 | I/O | External Data Bit. |
| P8 | DATA29 | I/O | External Data Bit. |
| T14 | DATA3 | I/O | External Data Bit. |
| R7 | DATA30 | I/O | External Data Bit. |
| P7 | DATA31 | I/O | External Data Bit. |
| R14 | DATA4 | I/O | External Data Bit. |
| P14 | DATA5 | I/O | External Data Bit. |
| U13 | DATA6 | I/O | External Data Bit. |
| T13 | DATA7 | I/O | External Data Bit. |
| R13 | DATA8 | I/O | External Data Bit. |
| P13 | DATA9 | I/O | External Data Bit. |
| C11 | DEVSELN | I/O | PCI Device Select Signal. Active Low. |
| R16 | ECSN0 | O | External I/O Device Chip Select. Active Low. |
| T16 | ECSN1 | O | External I/O Device Chip Select. Active Low. |
| U16 | ECSN2 | O | External I/O Device Chip Select. Active Low. |
| T17 | EROEN/ WRSTPLS | O/I | ROM/SRAM/FLASH and External I/O Output Enable. Active Low. WRSTO Polarity Select. WRSTPLS = 0, WRSTO = Active High; WRSTPLS = 1, Active Low. |
| M17 | ERWEN0/ TESTACK | O | External I/O and ROM/SRAM/FLASH Write Byte Enable. Active Low. |
| N17 | ERWEN1/ TESTREQB | O | External I/O and ROM/SRAM/FLASH Write Byte Enable. Active Low. |
| P17 | ERWEN2/ TESTREQA | O | External I/O and ROM/SRAM/FLASH Write Byte Enable. Active Low. |

Note:

1. O = Output.

I/O = Bidirectional.

O/I = Output in normal mode; input pin during reset.

| Pin Number | Pin Name | Type ⁽¹⁾ | Pin Function |
|------------|-----------------------|---------------------|--|
| R17 | ERWEN3/ TICTESTENN | O | External I/O and ROM/SRAM/FLASH Write Byte Enable. Active Low. |
| P16 | EWAITN | I | External Wait. Active Low. |
| D10 | FRAMEN | I/O | PCI Bus Frame Signal. Active Low. |
| A1 | GND | Gnd | Signal Ground. |
| G7 | GND | Gnd | Signal Ground. |
| G8 | GND | Gnd | Signal Ground. |
| G9 | GND | Gnd | Signal Ground. |
| G10 | GND | Gnd | Signal Ground. |
| G11 | GND | Gnd | Signal Ground. |
| H8 | GND | Gnd | Signal Ground. |
| H9 | GND | Gnd | Signal Ground. |
| H10 | GND | Gnd | Signal Ground. |
| H11 | GND | Gnd | Signal Ground. |
| J8 | GND | Gnd | Signal Ground. |
| J9 | GND | Gnd | Signal Ground. |
| J10 | GND | Gnd | Signal Ground. |
| J11 | GND | Gnd | Signal Ground. |
| K8 | GND | Gnd | Signal Ground. |
| K9 | GND | Gnd | Signal Ground. |
| K10 | GND | Gnd | Signal Ground. |
| K11 | GND | Gnd | Signal Ground. |
| L8 | GND | Gnd | Signal Ground. |
| L9 | GND | Gnd | Signal Ground. |
| L10 | GND | Gnd | Signal Ground. |
| L11 | GND | Gnd | Signal Ground. |
| C4 | GNT1N | O | PCI Bus Grant 2. Active Low. Output for Host Bridge Mode and Guest Bridge Mode. |
| C3 | GNT2N | O | PCI Bus Grant 2. Active Low. Output for Host Bridge Mode. Not Used in Guest Bridge Mode. |
| C2 | GNT3N | O | PCI Bus Grant 3. Active Low. Output for Host Bridge Mode. Not Used in Guest Bridge Mode. |
| G17 | GPIO0/EINT0 | I/O | General Purpose I/O Pin. External Interrupt Request Pin. |
| G16 | GPIO1/EINT1 | I/O | General Purpose I/O Pin. External Interrupt Request Pin. |
| K17 | GPIO10 | I/O | General Purpose I/O Pin. |
| K16 | GPIO11 | I/O | General Purpose I/O Pin. |
| K15 | GPIO12 | I/O | General Purpose I/O Pin. |
| K14 | GPIO13 | I/O | General Purpose I/O Pin. |
| L17 | GPIO14 | I/O | General Purpose I/O Pin. |

Note:

1. Gnd = Ground.

I = Input.

O = Output.

I/O = Bidirectional.

| Pin Number | Pin Name | Type ⁽¹⁾ | Pin Function |
|------------|-------------|---------------------|---|
| L16 | GPIO15 | I/O | General Purpose I/O Pin. |
| H17 | GPIO2/EINT2 | I/O | General Purpose I/O Pin. External Interrupt Request Pin. |
| H16 | GPIO3/EINT3 | I/O | General Purpose I/O Pin. External Interrupt Request Pin. |
| H15 | GPIO4/TOUT0 | I/O | General Purpose I/O Pin. Timer 0 Output Pin. |
| H14 | GPIO5/TOUT1 | I/O | General Purpose I/O Pin. Timer 1 Output Pin. |
| J17 | GPIO6 | I/O | General Purpose I/O Pin. |
| J16 | GPIO7 | I/O | General Purpose I/O Pin. |
| J15 | GPIO8 | I/O | General Purpose I/O Pin. |
| J14 | GPIO9 | I/O | General Purpose I/O Pin. |
| D7 | IDSEL | I | Initialization Device Select. Active High. |
| A9 | IRDYN | I/O | PCI Initiator Ready Signal. Active Low. |
| F1 | ISET | I | Set PHY Transmit Output Current. Connect to Ground with 3.01k Ω 1% Resistor. |
| B17 | L1LED0 | O | LAN Port 1 LED Programmable Indicator 0. Active Low. |
| B16 | L1LED1 | O | LAN Port 1 LED Programmable Indicator 1. Active Low. |
| C17 | L2LED0 | O | LAN Port 2 LED Programmable Indicator 0. Active Low. |
| C16 | L2LED1 | O | LAN Port 2 LED Programmable Indicator 1. Active Low. |
| D17 | L3LED0 | O | LAN Port 3 LED Programmable Indicator 0. Active Low. |
| D16 | L3LED1 | O | LAN Port 3 LED Programmable Indicator 1. Active Low. |
| E17 | L4LED0 | O | LAN Port 4 LED Programmable Indicator 0. Active Low. |
| E16 | L4LED1 | O | LAN Port 4 LED Programmable Indicator 1. Active Low. |
| H4 | LANRXM1 | I | LAN Port 1 PHY Receive Signal – (differential). |
| J4 | LANRXM2 | I | LAN Port 2 PHY Receive Signal – (differential). |
| K4 | LANRXM3 | I | LAN Port 3 PHY Receive Signal – (differential). |
| L4 | LANRXM4 | I | LAN Port 4 PHY Receive Signal – (differential). |
| H3 | LANRXP1 | I | LAN Port 1 PHY Receive Signal + (differential). |
| J3 | LANRXP2 | I | LAN Port 2 PHY Receive Signal + (differential). |
| K3 | LANRXP3 | I | LAN Port 3 PHY Receive Signal + (differential). |
| L3 | LANRXP4 | I | LAN Port 4 PHY Receive Signal + (differential). |
| H2 | LANTXM1 | O | LAN Port 1 PHY Transmit Signal – (differential). |
| J2 | LANTXM2 | O | LAN Port 2 PHY Transmit Signal – (differential). |
| K2 | LANTXM3 | O | LAN Port 3 PHY Transmit Signal – (differential). |
| L2 | LANTXM4 | O | LAN Port 4 PHY Transmit Signal – (differential). |
| H1 | LANTXP1 | O | LAN Port 1 PHY Transmit Signal + (differential). |
| J1 | LANTXP2 | O | LAN Port 2 PHY Transmit Signal + (differential). |
| K1 | LANTXP3 | O | LAN Port 3 PHY Transmit Signal + (differential). |
| L1 | LANTXP4 | O | LAN Port 4 PHY Transmit Signal + (differential). |
| E4 | M66EN | I | PCI 66 MHz Enable. |
| D2 | MPCIACTN | O | MiniPCI Active Signal. Active Low. |
| A16 | PAD0 | I/O | PCI Address and Data 0. |

Note:

1. I = Input.

O = Output.

I/O = Bidirectional.

| Pin Number | Pin Name | Type ⁽¹⁾ | Pin Function |
|------------|----------|---------------------|--|
| A15 | PAD1 | I/O | PCI Address and Data 1. |
| B13 | PAD10 | I/O | PCI Address and Data 10. |
| D13 | PAD11 | I/O | PCI Address and Data 11. |
| A12 | PAD12 | I/O | PCI Address and Data 12. |
| C12 | PAD13 | I/O | PCI Address and Data 13. |
| B12 | PAD14 | I/O | PCI Address and Data 14. |
| D12 | PAD15 | I/O | PCI Address and Data 15. |
| C9 | PAD16 | I/O | PCI Address and Data 16. |
| A8 | PAD17 | I/O | PCI Address and Data 17. |
| D9 | PAD18 | I/O | PCI Address and Data 18. |
| B8 | PAD19 | I/O | PCI Address and Data 19. |
| C15 | PAD2 | I/O | PCI Address and Data 2. |
| D8 | PAD20 | I/O | PCI Address and Data 20. |
| A7 | PAD21 | I/O | PCI Address and Data 21. |
| C7 | PAD22 | I/O | PCI Address and Data 22. |
| B7 | PAD23 | I/O | PCI Address and Data 23. |
| C6 | PAD24 | I/O | PCI Address and Data 24. |
| B6 | PAD25 | I/O | PCI Address and Data 25. |
| D6 | PAD26 | I/O | PCI Address and Data 26. |
| A5 | PAD27 | I/O | PCI Address and Data 27. |
| C5 | PAD28 | I/O | PCI Address and Data 28. |
| B5 | PAD29 | I/O | PCI Address and Data 29. |
| B15 | PAD3 | I/O | PCI Address and Data 3. |
| D5 | PAD30 | I/O | PCI Address and Data 30. |
| A4 | PAD31 | I/O | PCI Address and Data 31. |
| D15 | PAD4 | I/O | PCI Address and Data 4. |
| A14 | PAD5 | I/O | PCI Address and Data 5. |
| C14 | PAD6 | I/O | PCI Address and Data 6. |
| B14 | PAD7 | I/O | PCI Address and Data 7. |
| A13 | PAD8 | I/O | PCI Address and Data 8. |
| C13 | PAD9 | I/O | PCI Address and Data 9. |
| C8 | PAR | I/O | PCI Parity. |
| D3 | PBMS | I | PCI Bridge Mode Select. '1' = Host Bridge Mode. '0' = Guest Bridge Mode. |
| D4 | PCLK | I | PCI Bus Clock. |
| A2 | PCLKOUT0 | O | PCI Clock Output 0. |
| B1 | PCLKOUT1 | O | PCI Clock Output 1. |
| C1 | PCLKOUT2 | O | PCI Clock Output 2. |
| D1 | PCLKOUT3 | O | PCI Clock Output 3. |
| B11 | PERRN | I/O | PCI Parity Error Signal. Active Low. |
| A3 | PRSTN | I | PCI Reset. Active Low. |

Notes:

1. I = Input.
 O = Output.
 I/O = Bidirectional.

| Pin Number | Pin Name | Type ⁽¹⁾ | Pin Function |
|------------|---------------------|---------------------|--|
| P15 | RCSN0 | O | ROM/SRAM/FLASH Chip Select. Active Low. |
| R15 | RCSN1 | O | ROM/SRAM/FLASH Chip Select. Active Low. |
| B4 | REQ1N | I | PCI Bus Request 1. Active Low. Input for Host Bridge Mode and Guest Bridge Mode. |
| B3 | REQ2N | I | PCI Bus Request 2. Active Low. Input for Host Bridge Mode, Not Used in Guest Bridge Mode. |
| B2 | REQ3N | I | PCI Bus Request 3. Active Low. Input for Host Bridge Mode, Not Used in Guest Bridge Mode. |
| A17 | RESETN | I | KS8695P Chip Reset. Active Low. |
| T5 | SDCASN | O | SDRAM Column Address Strobe. Active Low. |
| P5 | SDCSN0 | O | SDRAM Chip Select. Active Low Chip Select Pins for SDRAM. |
| R4 | SDCSN1 | O | SDRAM Chip Select. Active Low Chip Select Pins for SDRAM. |
| T7 | SDICLK | I | SDRAM Clock In. |
| U7 | SDOCLK | O | System/SDRAM Clock Out. |
| U6 | SDQM0 | O | SDRAM Data Input/Output Mask. |
| T6 | SDQM1 | O | SDRAM Data Input/Output Mask. |
| R6 | SDQM2 | O | SDRAM Data Input/Output Mask. |
| P6 | SDQM3 | O | SDRAM Data Input/Output Mask. |
| R5 | SDRASN | O | SDRAM Row Address Strobe. Active Low. |
| U5 | SDWEN | O | SDRAM Write Enable. Active Low. |
| A10 | SERRN | O | PCI System Error Signal. Active Low. |
| D11 | STOPN | I/O | PCI Stop Signal. Active Low. |
| G14 | TCK | I | JTAG Test Clock. |
| F14 | TDI | I | JTAG Test Data In. |
| F15 | TDO | O | JTAG Test Data Out. |
| M4 | TEST1 | I | PHY Test Pin (factory reserved test signal). |
| F4 | TEST2 | I | PHY Test Pin (factory reserved test signal). |
| F17 | TESTEN | I | Chip Test Enable (factory reserved test signal). Must be connected to GND for normal operation |
| G15 | TMS | I | JTAG Test Mode Select |
| C10 | TRDYN | I/O | PCI Target Ready Signal. Active Low. |
| F16 | TRSTN | I | JTAG Test Reset. Active Low. |
| M14 | UCTSN/ BISTEN | I | UART Data Set Ready. Active Low. BIST Enable (factory reserved test signal). |
| L15 | UDCDN/ SCANEN | I | UART Data Carrier Detect. Scan Enable (factory reserved test signal). |
| M16 | UDSRN | I | UART Data Set Ready. Active Low. |
| N15 | UDTRN/ DBGENN | O/I | UART Data Terminal Ready. Active Low. Debug Enable (factory reserved test . signal) |
| L14 | URIN/TSTRST | I | UART Ring Indicator/Chip Test Reset (factory reserved test signal). |
| M15 | URTSN/ CPUCLKSEL | O/I | UART Request to Send/CPU Clock Select. |

Note:

1. I = Input.

O = Output.

I/O = Bidirectional.

O/I = Output in normal mode; input pin during reset.

| Pin Number | Pin Name | Type ⁽¹⁾ | Pin Function |
|------------|----------|---------------------|--|
| N16 | URXD | I | UART Receive Data. |
| N14 | UTXD | O | UART Transmit Data. |
| E7 | VDD1.8 | P | 1.8V Digital Core V _{DD} . |
| E8 | VDD1.8 | P | 1.8V Digital Core V _{DD} . |
| E9 | VDD1.8 | P | 1.8V Digital Core V _{DD} . |
| E10 | VDD1.8 | P | 1.8V Digital Core V _{DD} . |
| F7 | VDD1.8 | P | 1.8V Digital Core V _{DD} . |
| F8 | VDD1.8 | P | 1.8V Digital Core V _{DD} . |
| F9 | VDD1.8 | P | 1.8V Digital Core V _{DD} . |
| F10 | VDD1.8 | P | 1.8V Digital Core V _{DD} . |
| M7 | VDD1.8 | P | 1.8V Digital Core V _{DD} . |
| M8 | VDD1.8 | P | 1.8V Digital Core V _{DD} . |
| M9 | VDD1.8 | P | 1.8V Digital Core V _{DD} . |
| H12 | VDD1.8 | P | 1.8V Digital Core V _{DD} . |
| H13 | VDD1.8 | P | 1.8V Digital Core V _{DD} . |
| J12 | VDD1.8 | P | 1.8V Digital Core V _{DD} . |
| J13 | VDD1.8 | P | 1.8V Digital Core V _{DD} . |
| K12 | VDD1.8 | P | 1.8V Digital Core V _{DD} . |
| K13 | VDD1.8 | P | 1.8V Digital Core V _{DD} . |
| N7 | VDD1.8 | P | 1.8V Digital Core V _{DD} . |
| N8 | VDD1.8 | P | 1.8V Digital Core V _{DD} . |
| N9 | VDD1.8 | P | 1.8V Digital Core V _{DD} . |
| E11 | VDD3.3 | P | 3.3V Digital I/O Circuitry V _{DD} . |
| E12 | VDD3.3 | P | 3.3V Digital I/O Circuitry V _{DD} . |
| E13 | VDD3.3 | P | 3.3V Digital I/O Circuitry V _{DD} . |
| F11 | VDD3.3 | P | 3.3V Digital I/O Circuitry V _{DD} . |
| F12 | VDD3.3 | P | 3.3V Digital I/O Circuitry V _{DD} . |
| F13 | VDD3.3 | P | 3.3V Digital I/O Circuitry V _{DD} . |
| G12 | VDD3.3 | P | 3.3V Digital I/O Circuitry V _{DD} . |
| G13 | VDD3.3 | P | 3.3V Digital I/O Circuitry V _{DD} . |
| L12 | VDD3.3 | P | 3.3V Digital I/O Circuitry V _{DD} . |
| L13 | VDD3.3 | P | 3.3V Digital I/O Circuitry V _{DD} . |
| M10 | VDD3.3 | P | 3.3V Digital I/O Circuitry V _{DD} . |
| M11 | VDD3.3 | P | 3.3V Digital I/O Circuitry V _{DD} . |
| M12 | VDD3.3 | P | 3.3V Digital I/O Circuitry V _{DD} . |
| M13 | VDD3.3 | P | 3.3V Digital I/O Circuitry V _{DD} . |
| N10 | VDD3.3 | P | 3.3V digital I/O Circuitry V _{DD} . |
| N11 | VDD3.3 | P | 3.3V Digital I/O Circuitry V _{DD} . |
| N12 | VDD3.3 | P | 3.3V Digital I/O Circuitry V _{DD} . |
| N13 | VDD3.3 | P | 3.3V Digital I/O Circuitry V _{DD} . |

Notes:

1. P = Power supply.
I = Input.
O = Output.

| Pin Number | Pin Name | Type ⁽¹⁾ | Pin Function |
|------------|-------------------|---------------------|---|
| E5 | VDDA1.8 | P | 1.8V Analog V _{DD} . |
| E6 | VDDA1.8 | P | 1.8V Analog V _{DD} . |
| F5 | VDDA1.8 | P | 1.8V Analog V _{DD} . |
| F6 | VDDA1.8 | P | 1.8V Analog V _{DD} . |
| G5 | VDDA1.8 | P | 1.8V Analog V _{DD} . |
| G6 | VDDA1.8 | P | 1.8V Analog V _{DD} . |
| H5 | VDDA1.8 | P | 1.8V Analog V _{DD} . |
| H6 | VDDA1.8 | P | 1.8V Analog V _{DD} . |
| J5 | VDDA1.8 | P | 1.8V Analog V _{DD} . |
| J6 | VDDA1.8 | P | 1.8V Analog V _{DD} . |
| K5 | VDDA3.3 | P | 3.3V Analog V _{DD} . |
| K6 | VDDA3.3 | P | 3.3V Analog V _{DD} . |
| L5 | VDDA3.3 | P | 3.3V Analog V _{DD} . |
| L6 | VDDA3.3 | P | 3.3V Analog V _{DD} . |
| M5 | VDDA3.3 | P | 3.3V Analog V _{DD} . |
| M6 | VDDA3.3 | P | 3.3V Analog V _{DD} . |
| N5 | VDDA3.3 | P | 3.3V Analog V _{DD} . |
| N6 | VDDA3.3 | P | 3.3V Analog V _{DD} . |
| F2 | WANFXSD | I | WAN Fiber Signal Detect. |
| G4 | WANRXM | I | WAN PHY Receive Signal – (differential). |
| G3 | WANRXP | I | WAN PHY Receive Signal + (differential). |
| G2 | WANTXM | O | WAN PHY Transmit Signal – (differential). |
| G1 | WANTXP | O | WAN PHY Transmit Signal + (differential). |
| E15 | WLED0/ B0SIZE0 | O/I | WAN LED Programmable Indicator 0. Bank 0 Size Bit 0. |
| E14 | WLED1/ B0SIZE1 | O/I | WAN LED Programmable Indicator 1. Bank 0 Size Bit 1. |
| U17 | WRSTO | O | Watchdog Timer Reset Output. When EROEN/WRSTPLS = 0, Active High. When EROEN/WRSTPLS = 1, Active Low. |
| E1 | XCLK1 | I | External Clock In. |
| E2 | XCLK2 | I | External Clock In (negative polarity). |

Notes:

1. P = Power supply.

I = Input.

O = Output.

O/I = Output in normal mode; input pin during reset.

Pin Configuration

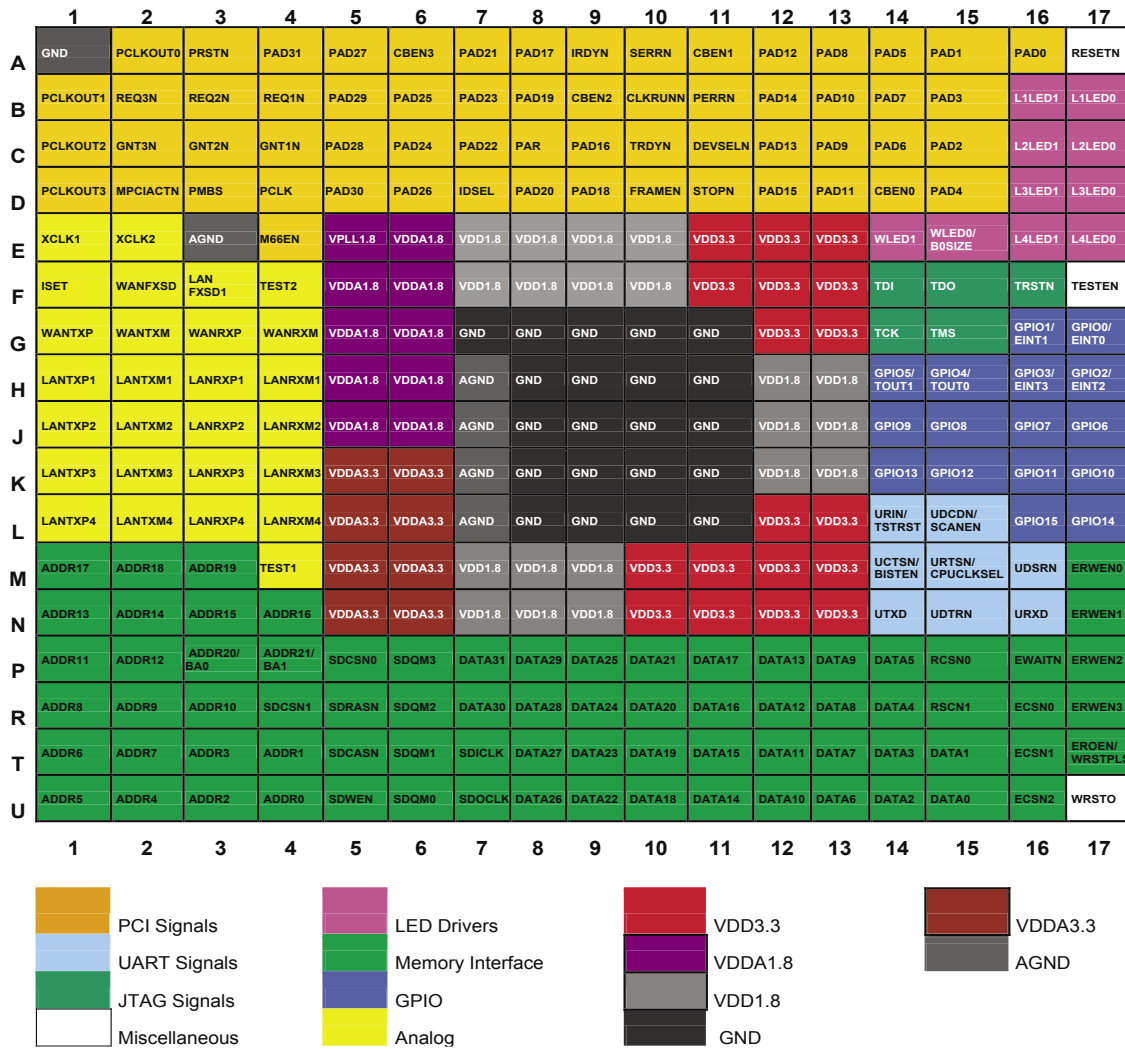


Figure 2. KS8695P Pin Mapping (Top View)

Functional Description

Introduction

Micrel's KS8695P, a member of the CENTAUR line of integrated processors, is a high-performance router-on-a-chip solution for Ethernet and 802.11 a/g/b based embedded systems. Designed for use in communication's routers, it integrates a PCI to AHB bridge solution for interfacing with 32-bit PCI, miniPCI, and cardbus devices. The KS8695P combines a proven third generation 5-port managed switch, an ARM9 RISC processor with MMU, and five physical layer transceivers (PHYs) including their corresponding MAC units with Micrel's XceleRouter technology.

The KS8695P is built around the 16/32-bit ARM9 RISC processor, which is a scalable, high-performance, microprocessor developed for highly integrated system-on-a-chip applications. It also offers a configurable 8KB I-cache and 8KB D-cache that reduces memory access latency for high-performance applications. The simple, elegant, and fully static design of the KS8695P is especially suitable for cost-effective, power-sensitive applications.

The KS8695P contains five 10/100 PHYs: four are for the local area network (LAN) and one is for the wide area network (WAN). Connected to the PHYs are five corresponding MAC units with an integrated Layer 2 managed switch. The combining of the switch and the analog PHYs make the KS8695P an extremely prudent solution for SOHO router applications, saving both board space and BOM costs. The Layer 2 switch contains a 16Kx32 SRAM on-chip memory for frame buffering. The embedded frame buffer memory is designed with a 1.4Gbps on-chip memory bus. This allows the KS8695P to perform full non-blocking frame switching and/or routing on the fly for many applications

For the media interface, the KS8695P supports 10BASE-T and 100BASE-TX, as specified by the IEEE 802.3 standard, and 100 BASE-FX on the WAN port and on one LAN port

The KS8695P supports two modes of operation in the PCI bus environment: host bridge mode and guest bridge mode. In the host bridge mode, the ARM9 processor acts as the host of the entire system. It configures other PCI devices and coordinates their transactions, including initiating transactions between the PCI devices and AHB bus subsystem. An on-chip PCI arbiter is included to determine the PCI bus ownership among PCI master devices. In host bridge mode, all I/O registers, including those for the embedded switch, are configured by the ARM9 processor through the on-chip AMBA bus interface.

In guest bridge mode, all of the I/O registers are programmed by either the external host CPU on the PCI bus or the local ARM9 host processor through the AMBA bus. The KS8695P functions as a slave on the PCI bus with the on-chip PCI arbiter disabled. The KS8695PX can be configured by either the ARM9 CPU or the PCI host CPU. In both cases, the KS8695P memory subsystem is accessible from either the PCI host or the ARM9 CPU. Communications between the external host CPU and the ARM9 is accomplished through message passing or through shared memory.

CPU Features

- 166MHz ARM9 RISC processor core
- On-chip AMBA bus 2.0 interfaces
- 16-bit thumb programming to relax memory requirement
- 8KB I-cache and 8KB D-cache
- Little-endian mode supported
- Configurable memory management unit
- Supports reduced CPU and system clock speed for power savings

PCI to AHB Bridge Features

- Support 33MHz, 32-bit data PCI bus
- Integrated PCI bridge support for interfacing with 32-bit miniPCI or cardbus devices
- Independent AHB and PCI clock speed
- Supports 125MHz AHB speed
- Supports PCI revision 2.1 protocols
- Supports AHB bus 2.0 interfaces
- Supports both regular and memory-mapped I/O on the PCI interface
- Integrated PCI arbiter with power-on option to enable or disable
- Support Round Robin arbitration with three external PCI devices and one internal device
- Supports AHB burst transfers up to 16 data words
- Configurable PCI registers by host CPU ARM9
- Supports bus mastership from PCI to AHB or AHB to PCI bus

Switch Engine

- 5-Port 10/100 integrated switch with one WAN and four LAN physical layer transceivers
- 16Kx32 on-chip SRAM for frame buffering
- 1.4Gbps on-chip memory bandwidth for wire-speed frame switching
- 10Mbps and 100Mbps modes of operation for both full and half duplex

Switch Engine (continued)

- Supports 802.1Q tag-based VLAN and port-based VLAN
- Supports 8.2,1p-based priority, DiffServ priority, and port-based priority
- Integrated address look-up engine, supports 1K absolute MAC addresses
- Automatic address learning, address aging, and address migration
- Broadcast storm protection
- Full-duplex IEEE 802.3x flow control
- Half-duplex back pressure flow control
- Supports IGMP snooping
- Spanning Tree Protocol support

Advanced Memory Controller Features

- Supports glueless connection to two banks of ROM/SRAM/FLASH memory with programmable 8/16/32 bit data bus and programmable access timing
- Supports glueless connection to two SDRAM banks with programmable 8/16/32-bit data bus and programmable RAS/CAS latency
- Supports three external I/O banks with programmable 8/16/32-bit data bus and programmable access timing
- Programmable system clock speed for power management
- Automatic address line mapping for 8/16/32-bit accesses on Flash, ROM, SRAM, and SDRAM interfaces

Direct Memory Access (DMA) Engines

- Independent MAC DMA engine with programmable burst mode for WAN port
- Independent MAC DMA engine with programmable burst mode for LAN ports
- Supports little-endian byte ordering for memory buffers and descriptors
- Contains large independent receive and transmit FIFOs (3KB receive/3KB transmit) for back-to-back packet receive, and guaranteed no under-run packet transmit
- Data alignment logic and scatter gather capability

Protocol Engine/XceleRouter Technology

- Supports IPv4 IP header/TCP/UDP packet checksum generation for host CPU offloading
- Supports IPv4 packet filtering based on checksum errors

Network Interface

- Features five MAC units and five PHY units
- Supports 10BASE-T and 100BASE-TX on all LAN ports and one WAN port. Also supports 100BASE-FX on the WAN port and on one LAN port
- Supports automatic CRC generation and checking
- Supports automatic error packet discard
- Supports IEEE 802.3 auto-negotiation algorithm of full-duplex and half-duplex operation for 10Mbps and 100Mbps
- Supports full-/half-duplex operation on PHY interfaces
- Fully compliant with IEEE 802.3 Ethernet standards
- IEEE 802.3 full-duplex flow control and half-duplex backpressure collision flow control
- Supports MDI/MDI-X auto-crossover

Peripherals

- Twenty-eight interrupt sources, including four external interrupt sources
- Normal or fast interrupt mode (IRQ, FIQ) supported
- Prioritized interrupt handling
- Sixteen programmable general purpose I/O. Pins individually configurable to input, output, or I/O mode for dedicated signals.
- Two programmable 32-bit timers with watchdog timer capability
- High-speed UART interface up to 115kbps

Other Features

- Integrated PLL to generate CPU and system clocks
- JTAG development interface for ICE connection
- 19mm x 19mm 289-pin PBGA
- 1.8V CMOS for core and 3.3V for I/O

System Level Hardware Interfaces

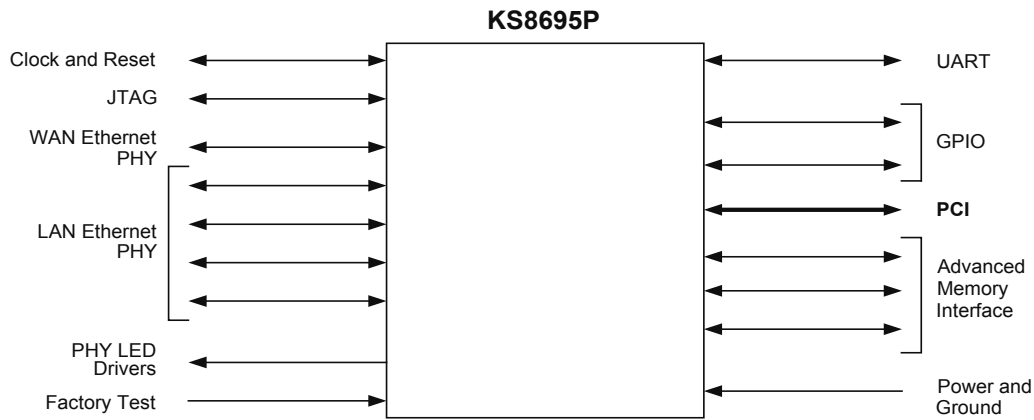


Figure 3. System Level Interfaces

At the system level the KS8695P features the following interfaces:

- Clock interface for crystal or external oscillator
- JTAG development interface
- One WAN Ethernet physical interface
- Four LAN Ethernet physical interfaces
- PHY LED drivers
- One high-speed UART interface
- Sixteen GPIO pins
- 33MHz, 32-bit PCI interface supporting three external masters
- Advanced memory interface
 - Programmable synchronous bus rate
 - Programmable asynchronous interface timing
 - Independently programmable data bus width for static and synchronous memory
 - Glueless connection to SDRAM
 - Glueless connection to flash memory or ROM
- Factory test
- Power and ground

Configuration Pins

The following pins are sampled as input during reset

| Configuration | Pin Name | Pin # | Setting |
|------------------------|-----------------|----------|--|
| Bank0 Flash Data Width | B0SIZE[1:0] | E14, E15 | '00' = reserved '01' = byte wide '10' = half word wide (16 bits) '11' = word wide (32 bits) |
| WRSTO Polarity | EROEN/WRSTPLS | U17 | '0' = active high '1' = active low |
| CPU Clock Select | URTSN/CPUCLKSEL | M15 | '0' = normal mode (PLL) '1' = bypass internal PLL |
| PCI Bridge Mode | PBMS | D3 | '0' = guest bridge mode '1' = host bridge mode |
| CPUCLKSEL | URTSN/CPUCLKSEL | M15 | '0' = normal operation '1' = factory reserved |
| Debug Enable | UDTRN/DBGENN | N15 | '0' = factory reserved |

Table 1. Configuration Pins

Following pins have second function as factory test of chip

| Configuration | Pin Name | Pin # | Setting |
|------------------|--------------------|-------|---|
| Chip Test Enable | TESTEN | F17 | '0' = normal operation '1' = factory reserved. Used for factory test of chip and affects all signals listed in this table. |
| | ERWEN0/TESTACK | M17 | |
| | ERWEN1/TESTREQB | N17 | |
| | ERWEN2/TESTREQA | P17 | |
| | ERWEN3/TICTESTTENN | R17 | |
| | UCTSN/BISTEN | M14 | |
| | UDCDN/SCANEN | L15 | |
| | URIN/TSTRST | L14 | |
| | TEST1 | M4 | |
| | TEST2 | F4 | |

Table 2. Configuration Pins

Reset

The KS8695P has a single reset input that can be driven by a system reset circuit or a simple power on reset circuit. The KS8695P also features a reset output (WRSTO) that can be used to reset other devices in the system. WRSTO can be configured as either an active high reset or an active low reset through a strap-in option on pin U17, as shown in Table 1. The KS8695P also has a built in watchdog timer. When the watchdog timer is programmed and the timer setting expires, the KS8695P resets itself and also asserts WRSTO to reset the other devices in the system. Figure 4 shows a typical system using the KS8695P WRSTO as the system reset.

Reset Circuit Diagram

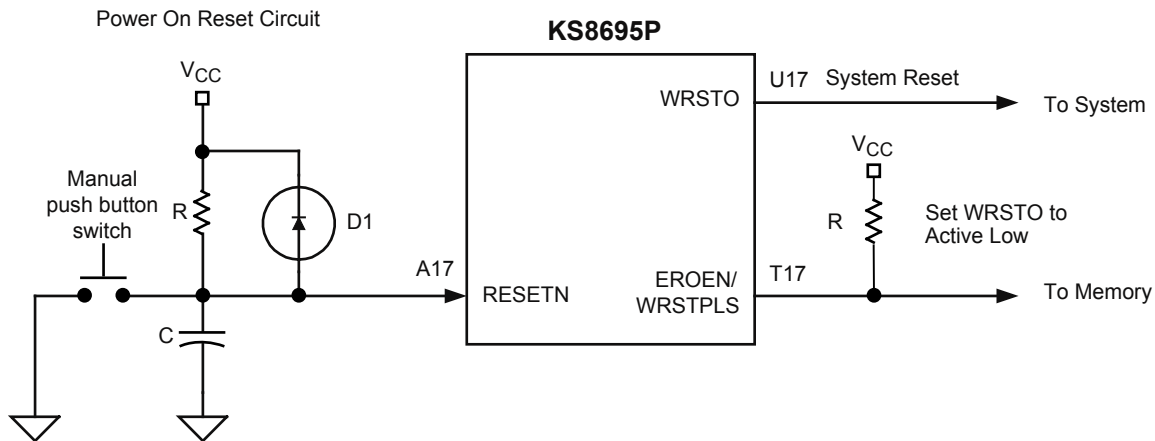


Figure 4. Example of a Reset Circuit

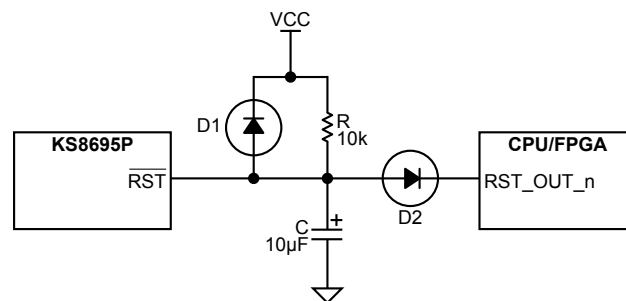


Figure 5. Recommended circuit for Interfacing with CPU/FPGA Reset

At power-on-reset, R, C, and D1 provide the necessary ramp rise time to reset the Micrel device. The reset out from CPU/FPGA provides warm reset after power up

System Clock

The clock to the KS8695P is supplied by either a 25MHz ± 50 ppm crystal or by an oscillator. If an oscillator is used, it must be connected to the XCLK1 input (pin E1) on the KS8695P. If a crystal is used, it must be connected with a circuit similar to the one shown below. The 25MHz input clock is used by an internal PLL to generate the programmable SDOCLK. SDOCLK is the system clock and can be programmed from 25MHz to 125MHz using the system clock and bus control register at offset 0x0004. The CPUCLKSEL strap-in option on pin M15 needs to be pulled low for normal operation. SDICLK is used to register the data read from the SDRAM back into the KS8695P. The system designer must ensure that SDRAM timing is met when routing SDOCLK back to SDICLK.

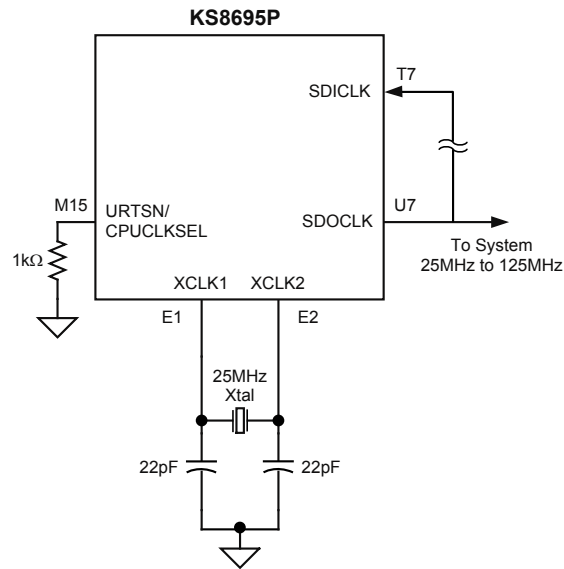


Figure 6. Typical Clock Circuit

Memory Interface

The KS8695P has a glueless interface for SDRAM and static memory, i.e. ROM, SRAM, and Flash. It supports up to two banks of static memory (Figure 7), up to two banks of SDRAM (Figure 8), and three banks of external I/O (Figure 9). The total address space for the KS8695P is 64MB. This includes SDRAM, static memory, external I/O, and the KS8695P's own 64KB of register space.

The memory interface for the SDRAM and static memory has a special automatic address mapping feature. This allows the designer to connect address bit 0 on the memory to ADDR[0] on the KS8695P and address bit 1 on the memory to ADDR[1] on the memory, regardless of whether the designer is trying to achieve word, half word, or byte addressing.

The KS8695P memory controller performs the address mapping internally. This permits the designer to use the maximum amount of address bits, instead of losing one or two bits because of address mapping. For external I/O, however, the designer still needs to take care of the address mapping (see Figure 9).

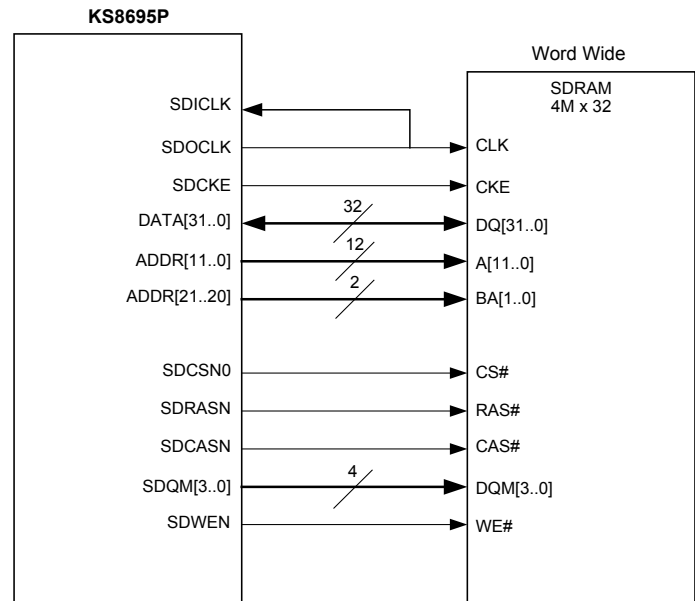
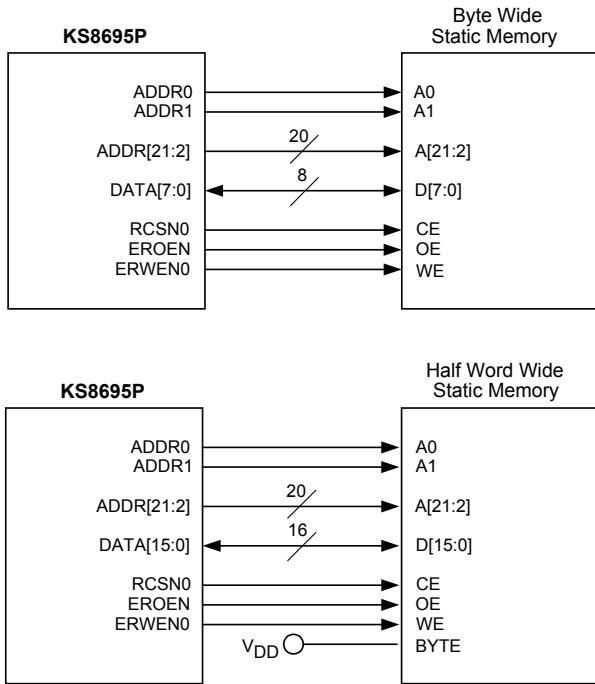
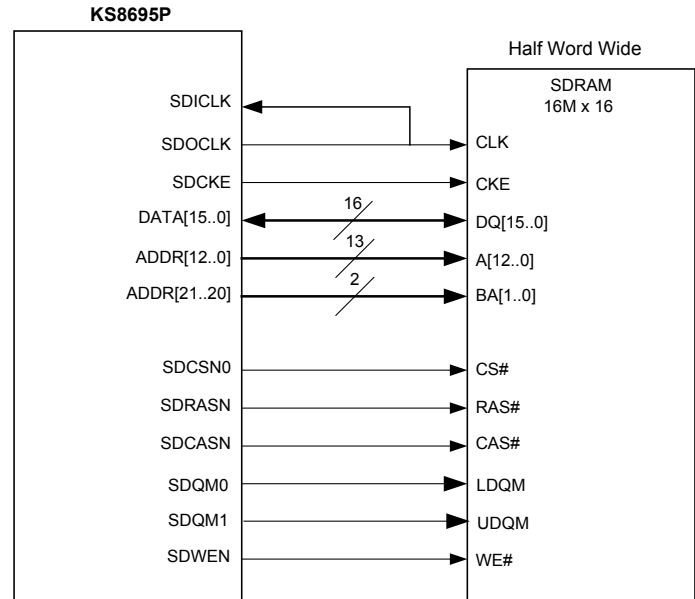


Figure 8. SDRAM Interface Examples

Figure 7. Static Memory Interface Examples

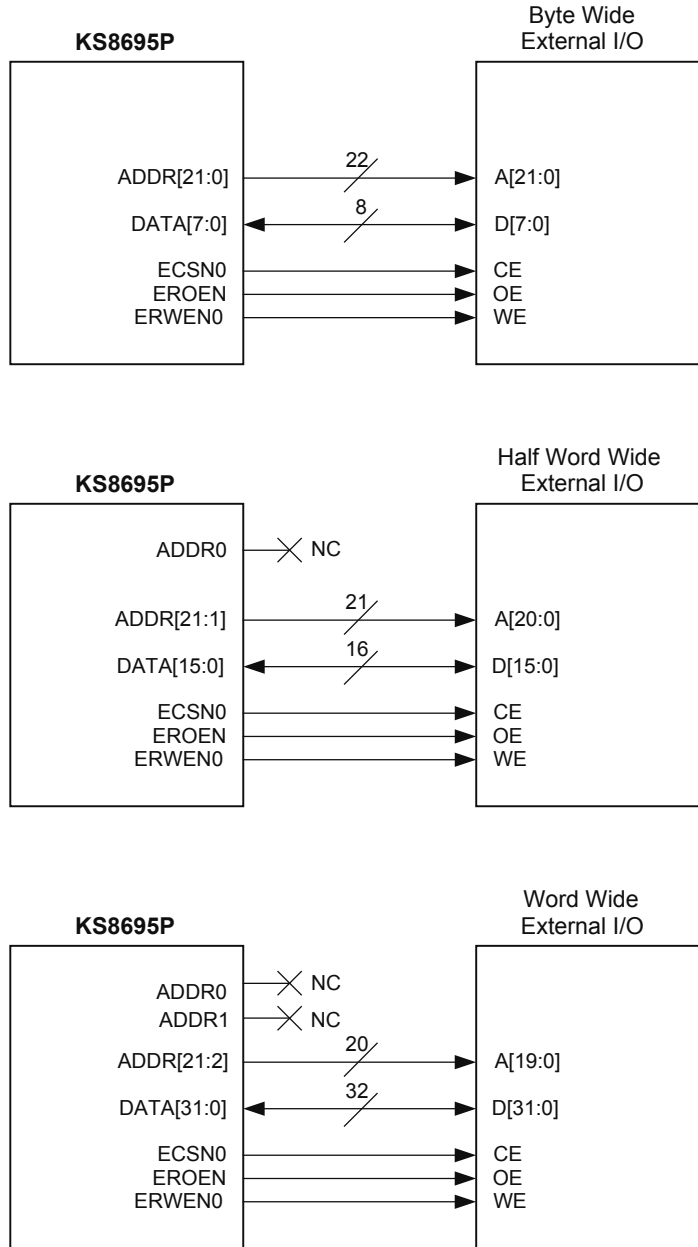


Figure 9. External I/O Interface Examples

KS8695P outputs ERWEN[3:0] as write strobes to byte wide, half-word wide, and word-wide memory port. The following figures show the most commonly implemented examples

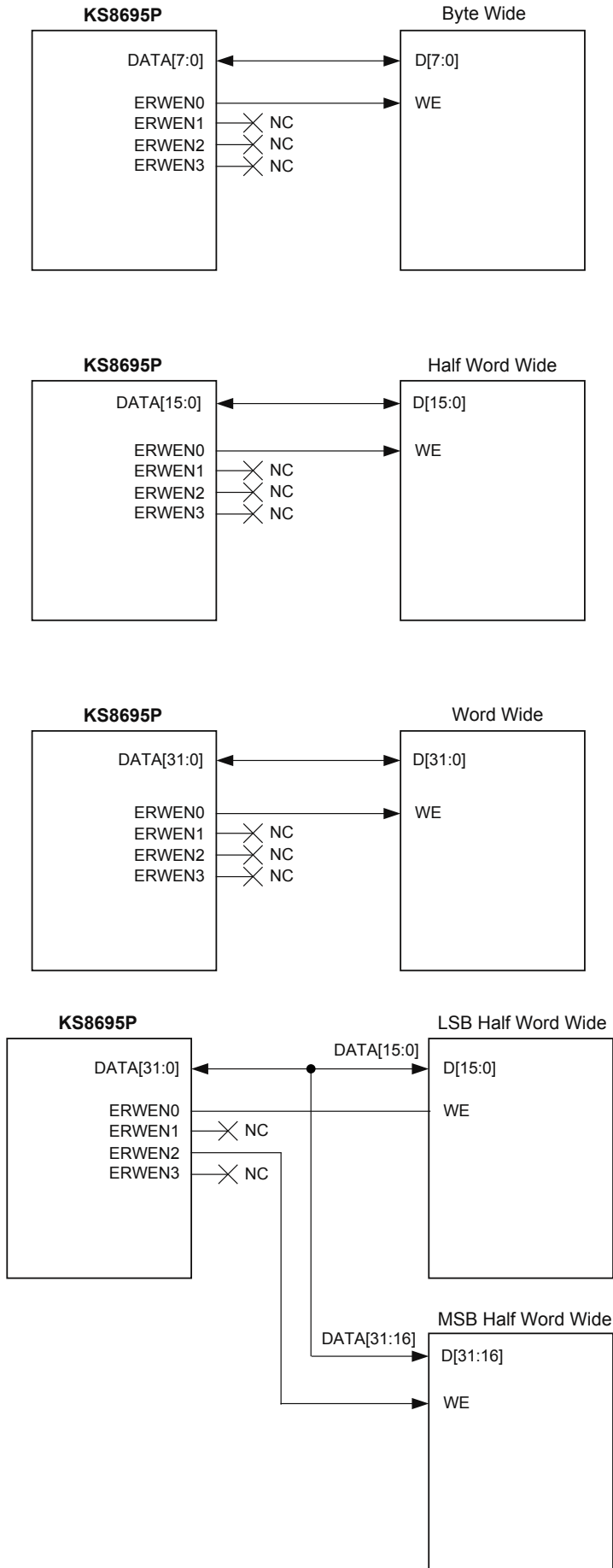


Figure 10 ERWEN[3:0] Interface Examples

Signal Descriptions by Group

Clock and Reset Pins

| Pin | Name | I/O Type ⁽¹⁾ | Description |
|-----|---------------------|-------------------------|--|
| E1 | XCLK1/ CPUCLK | I | External Clock In. This signal is used as the source clock for the transmit clock of the internal MAC and PHY. The clock frequency is 25MHz ±50ppm. The XCLK1 signal is also used as the reference clock signal for the internal PLL to generate the 125MHz internal system clock. |
| E2 | XCLK2 | I | External Clock In. Used with XCLK1 pin when another polarity of crystal is needed. This is unused for a normal clock input. |
| M15 | URTSN/ CPUCLKSEL | O/I | Normal Mode: UART request to send. Active low output. During reset: CPU clock select. Select CPU clock source. CPUCLKSEL=0 (normal mode), the internal PLL clock output is used as the CPU clock source. CPUCLKSEL=1 (factory reserved test signal). |
| A17 | RESETN | I | KS8695P chip reset. Active low input asserted for at least 256 system clock (40ns) cycles to reset the KS8695P. When in the reset state, all the output pins are tri-stated and all open drain signals are floating. |
| U17 | WRSTO | O | Watchdog timer reset output. This signal is asserted for at least 200ms if RESETN is asserted or when the internal watchdog timer expires. |
| T17 | EROEN/ WRSTPLS | O/I | Normal Mode: ROM/SRAM/FLASH and External I/O output enable. Active low. When asserted, this signal controls the output enable port of the specified device. During reset: Watchdog timer reset polarity setting. WRSTPLS=0, Active high; WRSTPLS=1, Active low. No default. |

JTAG Interface Pins

| Pin | Name | I/O Type ⁽¹⁾ | Description |
|-----|-------|-------------------------|------------------------------|
| G14 | TCK | I | JTAG test clock. |
| G15 | TMS | I | JTAG test mode select. |
| F14 | TDI | I | JTAG test data in. |
| F15 | TDO | O | JTAG test data out. |
| F16 | TRSTN | I | JTAG test reset. Active low. |

WAN Ethernet Physical Interface Pins

| Pin | Name | I/O Type ⁽¹⁾ | Description |
|-----|---------|-------------------------|---|
| G1 | WANTXP | O | WAN PHY transmit signal + (differential). |
| G2 | WANTXM | O | WAN PHY transmit signal – (differential). |
| G3 | WANRXP | I | WAN PHY receive signal + (differential). |
| G4 | WANRXM | I | WAN PHY receive signal – (differential). |
| G5 | WANFXSD | I | WAN fiber signal detect. Signal detect input when the WAN port is operated in 100BASE-FX 100Mb fiber mode. See Application Note 10. |

Note:

1. I = Input.

O = Output.

O/I = Output in normal mode; input pin during reset.

LAN Ethernet Physical Interface Pins

| Pin | Name | I/O Type ⁽¹⁾ | Description |
|----------------------|--|-------------------------|---|
| H1 J1 K1 L1 | LANTXP1 LANTXP2 LANTXP3 LANTXP4 | I | LAN Port[4:1] PHY transmit signal + (differential). |
| H2 J2 K2 L2 | LANTXM1 LANTXM2 LANTXM3 LANTXM4 | I | LAN Port[4:1] PHY transmit signal – (differential). |
| H3 J3 K3 L3 | LANRXP1 LANRXP2 LANRXP3 LANRXP4 | O | LAN Port[4:1] PHY receive signal + (differential). |
| H4 J4 K4 L4 | LANRXM1 LANRXM2 LANRXM3 LANRXM4 | O | LAN Port[4:1] PHY receive signal – (differential). |
| F1 | ISET | I | Set PHY transmit output current. Connect to ground through a 3.01kΩ 1% resistor. |
| F3 | LANFXSD1 | I | LAN fiber signal detect. Signal detect input when the LAN1 port is operated in 100BASE-FX 100Mb fiber mode. See Application Note 107. |

PHY LED Drivers

| Pin | Name | I/O Type ⁽¹⁾ | Description |
|--------------------------|--------------------------------------|-------------------------|---|
| E15 | WLED0/ B0SIZE0 | O/I | Normal Mode: WAN LED indicator 0. Programmable via WAN misc. Control register bits [2:0]. '000' = Speed; '001' = Link; '010' = Full/half duplex; '011' = Collision; '100' = TX/RX activity; '101' = Full-duplex collision; '110' = Link/Activity. During reset: Bank 0 Data Access Size. Bank 0 is used for the boot program. B0SIZE[1:0] are used to specify the size of the bank 0 data bus width as follows: '01' = one byte, '10' = half-word, '11' = one word, and '00' = reserved. |
| E14 | WLED1/ B0SIZE1 | O/I | Normal Mode: WAN LED indicator 1. Programmable via WAN Misc. Control register bits [6:4]. '000' = Speed; '001' = Link; '010' = Full/half duplex; '011' = Collision; '100' = TX/RX activity; '101' = Full-duplex collision; '110' = Link/Activity. During reset: Bank 0 data access size. Bank 0 is used for the boot program. B0SIZE[1:0] are used to specify the size of the bank 0 data bus width as follows: '01' = one byte, '10' = half-word, '11' = one word, and '00' = reserved. |
| B17 C17 D17 E17 | L1LED0 L2LED0 L3LED0 L4LED0 | O | LAN Port[4:1] LED indicator 0. Programmable via switch control 0 register bits [27:25]. '000' = Speed; '001' = Link; '010' = Full/half duplex; '011' = Collision; '100' = TX/RX activity; '101' = Full-duplex collision; '110' = Link/Activity. |
| B16 C16 D16 E16 | L1LED1 L2LED1 L3LED1 L4LED1 | O | LAN Port[4:1] LED indicator 1. Programmable via switch control 0 register bits [24:22]. '000' = Speed; '001' = Link; '010' = Full/half duplex; '011' = Collision; '100' = TX/RX activity; '101' = Full-duplex collision; '110' = Link/Activity. |

Note:

1. I = Input.

O = Output.

O/I = Output in normal mode; input pin during reset.

UART Pins

| Pin | Name | I/O Type ⁽¹⁾ | Description |
|-----|---------------------|-------------------------|--|
| N16 | URXD | I | UART receive data. |
| N14 | UTXD | O | UART transmit data. |
| N15 | UDTRN/ DBGENN | O/I | UART data terminal ready. Active low. DBGENN = 0 (factory reserved test signal) |
| M16 | UDSRN | I | UART data set ready. Active low. |
| M15 | URTSN/ CPUCLKSEL | O/I | Normal mode: UART request to send. Active low output. During reset: CPU clock select. Select CPU clock source. CPUCLKSEL=0 (normal mode), the internal PLL clock output is used as the CPU clock source. CPUCLKSEL=1 (factory reserved test signal). |
| M14 | UCTSN/ BISTEN | I | UART clear to send. BIST enable (factory reserved test signal). |
| L15 | UDCDN/ SCANEN | I | UART data carrier detect. Scan enable (factory reserved test signal). |
| L14 | URIN/ TSTRST | I | UART ring indicator. Chip test reset (factory reserved test signal). |

General Purpose I/O Pins

| Pin | Name | I/O Type ⁽¹⁾ | Description |
|-----|-----------------|-------------------------|--|
| G17 | GPIO0/ EINT0 | I/O | General purpose I/O pin. External interrupt request pin. |
| G16 | GPIO1/ EINT1 | I/O | General purpose I/O pin. External interrupt request pin. |
| H17 | GPIO2/ EINT2 | I/O | General purpose I/O pin. External interrupt request pin. |
| H16 | GPIO3/ EINT3 | I/O | General purpose I/O pin. External interrupt request pin. |
| H15 | GPIO4/ TOUT0 | I/O | General purpose I/O pin. Timer 0 output pin. |
| H14 | GPIO5/ TOUT1 | I/O | General purpose I/O pin. Timer 1 output pin. |
| J17 | GPIO6 | I/O | General purpose I/O pin. |
| J16 | GPIO7 | I/O | General purpose I/O pin. |
| J15 | GPIO8 | I/O | General purpose I/O pin. |
| J14 | GPIO9 | I/O | General purpose I/O pin. |
| K17 | GPIO10 | I/O | General purpose I/O pin. |
| K16 | GPIO11 | I/O | General purpose I/O pin. |
| K15 | GPIO12 | I/O | General purpose I/O pin. |
| K14 | GPIO13 | I/O | General purpose I/O pin. |
| L17 | GPIO14 | I/O | General purpose I/O pin. |
| L16 | GPIO15 | I/O | General purpose I/O pin. |
| A3 | PRSTN | I | PCI Reset. Active low. This signal is an input used to reset the KS8695P PCI logic. If the KS8695P is the host, use the RESETN signal to drive this input. If the KS8695P is a guest, use the system reset to drive this signal. |

Note:

1. I = Input.

O = Output.

I/O = Bidirectional.

O/I = Output in normal mode; input pin during reset.

General Purpose I/O Pins (continued)

| Pin | Name | I/O Type ⁽¹⁾ | Description |
|---|--|-------------------------|--|
| D4 | PCLK | I | PCI bus clock. This signal provides the timing for the PCI bus transactions. This signal is used to drive the PCI bus interface and the internal PCI logic. All PCI bus signals are sampled on the rising edges of the PCLK. PCLK can operate from 20MHz to 33MHz. For host mode, use PCLKOUT0 signal to drive this input. In guest mode, use the system PCI clock to drive this input. |
| C2 | GNT3N | O | PCI bus grant 3. Active low. In host bridge mode, this is an output signal from the internal PCI arbiter to grant PCI bus access to the device connected to REQ3N. In guest bridge mode, this signal is reserved. |
| C3 | GNT2N | O | PCI bus grant 2. Active low. In host bridge mode, this is an output signal from the internal PCI arbiter to grant PCI bus access to the device connected to REQ2N. In guest bridge mode, this signal is reserved. |
| C4 | GNT1N | O | PCI bus grant 1. Active low. In host bridge mode, this is an output signal from the internal PCI arbiter to grant PCI bus access to the device connected to REQ1N. In guest bridge mode, this signal is an output to indicate that the KS8695P is requesting to access the PCI bus as a PCI master. In guest bridge mode, this is basically the KS8695P's request output. |
| B2 | REQ3N | I | PCI bus request 3. Active low. In host bridge mode, this is an input signal from the external PCI device to request PCI bus access. In guest bridge mode, this signal is reserved. |
| B3 | REQ2N | I | PCI bus request 2. Active low. In host bridge mode, this is an input signal from the external PCI device to request PCI bus access. In guest bridge mode, this signal is reserved. |
| B4 | REQ1N | I | PCI bus request 1. Active low. In host bridge mode, this is an input signal from the external PCI device to request PCI bus access. In guest bridge mode, this is an input signal from an external PCI bus arbiter granting access to the bus. In guest bridge, this is basically the KS8695P's grant input. |
| A4 D5 B5 C5 A5 D6 B6 C6 B7 C7 A7 D8 B8 D9 A8 C9 D12 B12 C12 A12 D13 B13 C13 A13 B14 C14 A14 D15 B15 | PAD31 PAD30 PAD29 PAD28 PAD27 PAD26 PAD25 PAD24 PAD23 PAD22 PAD21 PAD20 PAD19 PAD18 PAD17 PAD16 PAD15 PAD14 PAD13 PAD12 PAD11 PAD10 PAD9 PAD8 PAD7 PAD6 PAD5 PAD4 PAD3 | I/O | 32-Bit PCI address and data. PCI bus transactions consist of an address phase followed by one or more data phases. Address and data signals are multiplexed on the same pins. For a PCI write transaction, the source of the data is the KS8695P. For a PCI read transaction, the data source is the target. The KS8695P supports both read and write burst transactions. In the case of a read transaction, a special data turn around cycle is needed between the address phase and the data phase(s). |

Note:

1. I = Input.

O = Output.

I/O = Bidirectional.

General Purpose I/O Pins (continued)

| Pin | Name | I/O Type ⁽¹⁾ | Description |
|------------------------|----------------------------------|-------------------------|--|
| C15 A15 A16 | PAD2 PAD1 PAD0 | I/O | 32-Bit PCI address and data (continued from previous page). |
| A6 B9 A11 D14 | CBEN3 CBEN2 CBEN1 CBEN0 | I/O | PCI commands and byte enable. Active low. The PCI command and byte enable signals are multiplexed on the same pins. During the first clock cycle of a PCI transaction, the CBEN bus contains the command for the transaction. The PCI transaction consists of the address phases and one or more data phases. During the data phases of the transaction, the bus carries the byte enable for the current data phases. |
| C8 | PAR | I/O | Parity. PCI bus parity is even across PAD[31:0] and CBEN[3:0]. The KS8695P generates PAR during the address phase and write data phases as a bus master and during read data phases as a target. It checks for correct PAR during the read data phase as a bus master, during every address phase as a bus slave, and during write data phases as a target. |
| D10 | FRAMEN | I/O | PCI bus frame signal. Active low. FRAMEN is an indication of an active PCI bus cycle. It is asserted at the beginning of a PCI transaction, i.e. the address phase, and deasserted before the final transfer of the data phase of the transaction. |
| A9 | IRDYN | I/O | PCI initiator ready signal. Active low. This signal is asserted by a PCI master to indicate a valid data phase on the PAD bus during data phases of a write transaction. During a read transaction, it indicates that the master is ready to accept data from the target. A target monitors the IRDYN signal when a data phase is completed on any rising edge of the PCI clock when both IRDYN and TRDYN are asserted. Wait cycles are inserted until both IRDYN and TRDYN are asserted together. |
| C10 | TRDYN | I/O | PCI target ready signal. Active low. This signal is asserted by a PCI slave to indicate a valid data phase on the PAD bus during a read transaction. During a write transaction, it indicates that the slave is ready to accept data from the target. A PCI initiator monitors the TRDYN signal when a data phase is completed on any rising edge of the PCI clock when both IRDYN and TRDYN are asserted. Wait cycles are inserted until both IRDYN and TRDYN are asserted together. |
| C11 | DEVSELN | I/O | PCI device select signal. Active low. This signal is asserted when the KS8695P is selected as a target during a bus transaction. When the KS8695P is the initiator of the current bus access, it expects the target to assert DEVSELN within five PCI bus cycles, confirming the access. If the target does not assert DEVSELN within the required bus cycles, the KS8695P aborts the bus cycle. To meet the timing requirement, the KS8695P asserts this signal in a medium speed decode timing. (two bus cycles). |
| D7 | IDSEL | I | Initialization device select. Active high. It is used as a chip select during configuration read and write transactions. |
| D11 | STOPN | I/O | PCI stop signal. Active low. This signal is asserted by the PCI target to indicate to the bus master that it is terminating the current transaction. The KS8695P responds to the assertion of STOPN when it is the bus master, either to disconnect, retry, or abort the transaction. |
| B11 | PERRN | I/O | PCI parity error signal. Active low. The KS8695P asserts PERRN when it checks and detects a bus parity error. When it generates the PAR output, the KS8695P monitors for any reported parity error on PERRN. When the KS8695P is the bus master and a parity error is detected, the KS8695P sets error bits in the control status registers. It completes the current data burst transaction, and then stops the operation. After the host clears the system error, the KS8695P continues its operation. |
| A10 | SERRN | O | PCI system error signal. Active low. If an address parity error is detected, the KS8695P asserts the SERRN signal two clocks after the failing address. |
| E4 | M66EN | I | PCI 66MHz enable. When asserted, this signal indicates the PCI bus segment is operating at 66MHz. This pin is mainly used in guest bridge mode when the PCLK is driven by an external host bridge. |

Note:

1. I = Input.

O = Output.

I/O = Bidirectional.

General Purpose I/O Pins (continued)

| Pin | Name | I/O Type ⁽¹⁾ | Description |
|-----|----------|-------------------------|--|
| D1 | PCLKOUT3 | O | PCI clock output 3. In host bridge mode driven as 33MHz In guest bridge mode, this signal is reserved |
| C1 | PCLKOUT2 | O | PCI clock output 2. In host bridge mode driven as 33MHz In guest bridge mode, this signal is reserved |
| B1 | PCLKOUT1 | O | PCI clock output 1. In host bridge mode driven as 33MHz In guest bridge mode, this signal is reserved |
| A2 | PCLKOUT0 | O | PCI clock output 0. In host bridge mode driven as 33MHz In guest bridge mode, this signal is reserved |
| B10 | CLKRUNN | I/O | This is a cardbus only signal. The CLKRUNN signal is used by portable cardbus devices to request that the system turn on the bus clock. Output is always active in cardbus and miniPCI modes. |
| D2 | MPCIACTN | O | MiniPCI active. This signal is asserted by the PCI device to indicate that its current function requires full system performance. MPCIACTN is an open drain output signal. In miniPCI mode, this signal is always low. |
| D3 | PBMS | I | PCI bridge mode select. This selects the operating mode for the PCI bridge. When PBMS is high, the host bridge mode is selected and the on-chip PCI bus arbiter is enabled. When PBMS is low, the guest bridge mode is selected and the on-chip arbiter is disabled. |

Advanced Memory Interface (SDRAM/ROM/FLASH/SRAM/EXTERNAL I/O)

| Pin | Name | I/O Type ⁽¹⁾ | Description |
|--|--|-------------------------|--|
| T7 | SDICLK | I | SDRAM Clock In: SDRAM clock input for the SDRAM memory controller interface. |
| U7 | SDOCLK | O | System/SDRAM Clock Out: Output of the internal system clock, it is also used as the clock signal for SDRAM interface. |
| P4 | ADDR21/BA1 | O | Address Bit 21/Bank Address Input 1: Address bit 21 for asynchronous accesses. Bank Address Input bit 1 for SDRAM accesses. |
| P3 | ADDR20/BA0 | O | Address Bit 20/Bank Address Input 0: Address bit 20 for asynchronous accesses. Bank Address Input bit 0 for SDRAM accesses. |
| M3 M2 M1 N4 N3 N2 N1 P2 P1 R3 R2 R1 T2 T1 U1 U2 T3 U3 T4 U4 | ADDR[19] ADDR[18] ADDR[17] ADDR[16] ADDR[15] ADDR[14] ADDR[13] ADDR[12] ADDR[11] ADDR[10] ADDR[9] ADDR[8] ADDR[7] ADDR[6] ADDR[5] ADDR[4] ADDR[3] ADDR[2] ADDR[1] ADDR[0] | O | Address Bus: The 22-bit address bus (including ADDR[21:20] above) covers 4M word memory space shared by ROM/SRAM/FLASH, SDRAM, and external I/O banks. During the SDRAM cycles, the internal address bus is used to generate RAS and CAS addresses for the SDRAM. The number of column address bits in the SDRAM banks can be programmed from 8 to 11 bits via the SDRAM control registers. ADDR[12:0] are the SDRAM address and ADDR[21:20] are the SDRAM bank address. During other cycles, the ADDR[21:0] is the byte address of the data transfer. For SDRAM and FLASH/ROM/SRAM, connect all address lines, i.e. A0 to A0, A1 to A1, etc. The memory controller automatically handles address line adjustments for the 8/16/32 bit accesses. For external I/O devices, the user needs to connect address lines for 8/16/32 bit accesses. |

Note:

1. I = Input.

O = Output.

I/O = Bidirectional.

Advanced Memory Interface (SDRAM/ROM/FLASH/SRAM/EXTERNAL I/O)

| Pin | Name | I/O Type ⁽¹⁾ | Description |
|--|--|-------------------------|---|
| P7 R7 P8 R8 T8 U8 P9 R9 T9 U9 P10 R10 T10 U10 P11 R11 T11 U11 P12 R12 T12 U12 P13 R13 T13 U13 P14 R14 T14 U14 T15 U15 | DATA[31] DATA[30] DATA[29] DATA[28] DATA[27] DATA[26] DATA[25] DATA[24] DATA[23] DATA[22] DATA[21] DATA[20] DATA[19] DATA[18] DATA[17] DATA[16] DATA[15] DATA[14] DATA[13] DATA[12] DATA[11] DATA[10] DATA[9] DATA[8] DATA[7] DATA[6] DATA[5] DATA[4] DATA[3] DATA[2] DATA[1] DATA[0] | I/O | External Data Bus. 32-Bit bi-directional data bus for data transfer. The KS8695P also supports 8-bit and 16-bit data bus widths. |
| R4 P5 | SDCSN[1] SDCSN[0] | O | SDRAM Chip Select: Active low chip select pins for SDRAM. The KS8695P supports up to two SDRAM banks. One SDCSN output is provided for each bank. |
| R5 | SDRASN | O | SDRAM Row Address Strobe: Active low. The row address strobe pin for SDRAM. |
| T5 | SDCASN | O | SDRAM Column Address Strobe: Active low. The column address strobe pin for SDRAM. |
| U5 | SDWEN | O | SDRAM Write Enable: Active low. The write enable signal for SDRAM. |
| P6 R6 T6 U6 | SDQM[3] SDQM[2] SDQM[1] SDQM[0] | O | SDRAM Data Input/Output Mask: Data input/output mask signals for SDRAM. The SDQM is sampled high and is an output mask signal for write accesses and an output enable signal for read accesses. Input data are masked during a write cycle. The SDQM0/1/2/3 correspond to DATA[7:0], DATA[15:8], DATA[23:16] and DATA[31:24], respectively. |
| U16 T16 R16 | ECSN[2] ECSN[1] ECSN[0] | O | External I/O Device Chip Select: Active low. Three external I/O banks are provided for external memory mapped I/O operations. Each I/O bank stores up to 16KB. The ECSNx signals indicate which of the three I/O banks is selected. |
| P16 | EWAITN | I | External Wait: Active low. This signal is asserted when an external I/O device or a ROM/SRAM/FLASH bank needs more access cycles than those defined in the corresponding control register. |
| R15 P15 | RCSN[1] RCSN[0] | O | ROM/SRAM/FLASH Chip Select: Active low. The KS8695P can access up to two external ROM/SRAM/FLASH memory banks. The RCSN pins can be controlled to map the CPU addresses into physical memory banks. |

Note:

1. I = Input.
O = Output.
I/O = Bidirectional.

| Pin | Name | I/O Type ⁽¹⁾ | Description |
|-----|-----------------------|-------------------------|---|
| T17 | EROEN/ WRSTPLS | O/I | Normal mode: External I/O and ROM/SRAM/FLASH output enable: Active low. When asserted, this signal controls the output enable port of the specified memory device. During reset: Watchdog timer reset polarity setting. WRSTPLS=0, active low; WRSTPLS = 1, active high. No default. |
| M17 | ERWEN0/ TESTACK | O | External I/O and ROM/SRAM/FLASH write byte enable: Active low. When asserted, the ERWENx controls the byte write enable of the memory device (except SDRAM). ARM CPU test signal (factory reserved test signal). |
| N17 | ERWEN1/ TESTREQB | O | External I/O and ROM/SRAM/FLASH write byte enable: Active low. When asserted, the ERWENx controls the byte write enable of the memory device (except SDRAM). ARM CPU test signal (factory reserved test signal). |
| P17 | ERWEN2/ TESTREQA | O | External I/O and ROM/SRAM/FLASH write byte enable: Active low. When asserted, the ERWENx controls the byte write enable of the memory device except SDRAM). ARM CPU test signal (factory reserved test signal). |
| R17 | ERWEN3/ TICTESTENN | O | External I/O and ROM/SRAM/FLASH write byte enable. Active low. When asserted, the ERWENx controls the byte write enable of the memory device (except SDRAM). ARM CPU test signal (factory reserved test signal). |
| E15 | WLED0/ BOSIZE0 | O/I | Normal mode: WAN LED indicator 0: Programmable via WAN misc. Control register bits [2:0]. 000 = Speed; 001 = Link; 010 = Full/half duplex; 011 = Collision; 100 = TX/RX activity; 101 = Full-duplex collision; 110 = Link/Activity. During reset: Bank 0 data access size. Bank 0 is used for the boot program. BOSIZE[1:0] are used to specify the size of the bank 0 data bus width as follows: '01' = one byte, '10' = half-word, '11' = one word, and '00' = reserved. |
| E14 | WLED1/ BOSIZE1 | O/I | Normal mode: WAN LED indicator 1: Programmable via WAN Misc. Control register bits [6:4]. 000 = Speed; 001 = Link; 010 = Full/half duplex; 011 = Collision; 100 = TX/RX activity; 101 = Full-duplex collision; 110 = Link/Activity. During reset: Bank 0 data access size. Bank 0 is used for the boot program. BOSIZE[1:0] are used to specify the size of the bank 0 data bus width as follows: '01' = one byte, '10' = half-word, '11' = one word, and '00' = reserved. |

Factory Test Pins

| Pin | Name | I/O Type ⁽¹⁾ | Description |
|-----|--------|-------------------------|---|
| F7 | TESTEN | I | Factory test signal. Pull-down or direct connect to GND required. |
| M4 | TEST1 | I | Factory test signal. No connect for normal operation. |
| F4 | TEST2 | I | Factory test signal. No connect for normal operation. |

Note:

1. I = Input.

O = Output.

O/I = Output in normal mode; input pin during reset.

Power and Ground Pins

| Pin | Name | I/O Type ⁽¹⁾ | Description |
|--|---------|-------------------------|------------------------------|
| E5 E6 F5 F6 G5 G6 H5 H6 J5 J6 | VDDA1.8 | P | 1.8V analog V_{DD} . |
| E7 E8 E9 E10 F7 F8 F9 F10 M7 M8 M9 H12 H13 J12 J13 K12 K13 N7 N8 N9 | VDD1.8 | P | 1.8V digital core V_{DD} . |
| K5 K6 L5 L6 M5 M6 N5 N6 | VDDA3.3 | P | 3.3V analog V_{DD} . |
| E11 E12 E13 F11 F12 F13 G12 G13 L12 L13 M10 M11 M12 M13 N10 N11 N12 N13 | VDD3.3 | P | 3.3V digital I/O V_{DD} . |

Note:

1. P = Power supply.

| Pin | Name | I/O Type ⁽¹⁾ | Description |
|--|------|-------------------------|----------------|
| E3 H7 J7 K7 L7 | AGND | Gnd | Analog Ground. |
| A1 G7 G8 G9 G10 G11 H8 H9 H10 H11 J8 J9 J10 J11 K8 K9 K10 K11 L8 L9 L10 L11 | GND | Gnd | Ground. |

Note:

1. Gnd = Ground.

Address Map and Register Description

Memory Map

Upon power up, the KS8695P memory map is configured as shown below.

| Address Range | Region | Description |
|-----------------------|--------|---|
| 0x03FF0000-0x03FFFFFF | 64KB | KS8695P System Configuration Register Space |
| 0x02000000-0x03FEFFFF | 32MB | Not Configured |
| 0x00000000-0x01FFFFFF | 32MB | Flash Bank 0 |

Memory Map Example

The default base address for the KS8695P system configuration registers is 0x03ff0000. After power up, the user is free to re-map the memory for their specific application. The following is an example of the memory space remapped for operation.

| Address Range | Region | Description |
|------------------------|--------|---|
| 0x03FF0000-0x03FFFFFF | 64KB | KS8695P System Configuration Register Space |
| 0x03E00000-0x03FEFFFF | 2MB | Disabled, Not Used |
| 0x03200000-0x036FFFFFF | 5MB | Space (External I/O) |
| 0x02C00000-0x031FFFFFF | 6MB | Reserved FLASH Space, Not Used |
| 0x02800000-0x02BFFFFFF | 4MB | FLASH |
| 0x02000000-0x027FFFFFF | 8MB | Disabled, Not Used |
| 0x00000000-0x01FFFFFF | 32MB | SDRAM |

Register Description

The KS8695P system configuration registers (SCRs) are located in a block of 64KB in the host memory address space. After power up and initialization, the user can remap the SCRs to a desired offset. The SCRs are 32 bits wide. They are 32 bit word-aligned and must be accessed using word instructions.

The AHB-PCI bridge configuration registers are also included in the SCRs. A subset of the AHB-PCI bridge configuration registers is also accessible to an external PCI host when the KS8695P is configured in PCI guest mode. Refer to the detailed Register Description document for additional information, including bit definitions. If you don't have this document, contact your local Micrel Field Application Engineer or salesperson.

| Address Range | Register Type | Register Type | Address Range |
|-----------------|------------------------------|----------------------|---------------------------|
| 0x0000 – 0x0004 | System Registers | System Configuration | 0x03FFFFFF – 0x03FEFFFF |
| 0x2000 – 0x2224 | PCI-AHB Bridge Configuration | External I/O Bank 2 | 0x03FEFFFF – 0x039FFFFFF |
| 0x4000 – 0x4040 | Memory Controller Interface | External I/O Bank 1 | 0x039FFFFFF – 0x035FFFFFF |
| 0x6000 – 0x60FC | WAN DMA | External I/O Bank 0 | 0x035FFFFFF – 0x031FFFFFF |
| 0x8000 – 0x80FC | LAN DMA | Not Used | 0x031FFFFFF – 0x02FFFFFF |
| 0xA000 – 0xA0FC | Reserved | Flash Bank 0 – 4MB | 0x02FFFFFF – 0x027FFFFFF |
| 0xE000 – 0xA0FC | UART Registers | Not Used | 0x027FFFFFF – 0x00FFFFFF |
| 0xE200 – 0xE234 | Interrupt Controller | SDRAM 16MB | 0x00FFFFFF – 0x00000000 |
| 0xE400 – 0xE410 | Timer Registers | | |
| 0xE600 – 0xE608 | General Purpose I/O | | |
| 0xE800 – 0xE850 | Switch Engine Configuration | | |
| 0xEA00 – 0xEA18 | Miscellaneous Registers | | |

Absolute Maximum Ratings⁽¹⁾

Supply Voltage

| | |
|--|-----------------|
| $(V_{DDA1.8}, V_{DD1.8})$ | -0.5V to +2.4V |
| $(V_{DDA3.3}, V_{DD3.3})$ | -0.5V to +4.0V |
| Input Voltage (all inputs) | -0.5V to +4.0V |
| Output Voltage (all outputs) | -0.5V to +4.0V |
| Lead Temperature (soldering, 10sec.) | 270°C |
| Pb (Lead) Free Temperature (soldering, 10sec.) | 260°C |
| Storage Temperature (T_S) | -55°C to +150°C |

Operating Ratings⁽²⁾

Supply Voltage

| | |
|--|----------------|
| $(V_{DDA1.8}, V_{DD1.8})$ | +1.7V to +1.9V |
| $(V_{DDA3.3}, V_{DD3.3})$ ⁽³⁾ | +3.0V to +3.6V |
| Ambient Temperature (T_A) | -0°C to +70°C |
| Junction Temperature (T_J) | 150°C |
| Package Thermal Resistance ⁽⁴⁾ | |
| PBGA (θ_{JA}) No Air Flow | 29.86°C/W |
| 1m/s | 21.86°C/W |
| 2m/s | 21.54°C/W |
| (θ_{JC}) No Air Flow | 8.34°C/W |

Electrical Characteristics⁽⁵⁾

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|--|-------------------------------|-----|-------|-----|---------|
| Total Supply Current (including TX output driver current) | | | | | | |
| 100BASE-TX Operation: All ports 100% Utilization, SDOCLK = 125MHz | | | | | | |
| I_{TX} | 100BASE-TX (Analog TX) | $V_{DDA3.3} = +3.3V$ | | 0.032 | | A |
| I_{RX} | 100BASE-TX (Analog RX) | $V_{DDA1.8} = +1.8V$ | | 0.072 | | A |
| I_{DDIO} | 100BASE-T (Digital I/O) | $V_{DD3.3} = +3.3V$ | | 0.033 | | A |
| I_{DDC} | 100BASE-T (Digital Core) | $V_{DD1.8} = +1.8V$ | | 0.235 | | A |
| 10BASE-TX Operation: All ports 100% Utilization, SDOCLK = 125MHz | | | | | | |
| I_{TX} | 10BASE-T (Analog TX) | $V_{DDA3.3} = +3.3V$ | | 0.030 | | A |
| I_{RX} | 10BASE-T (Analog RX) | $V_{DDA1.8} = +1.8V$ | | 0.072 | | A |
| I_{DDIO} | 10BASE-T (Digital I/O) | $V_{DD3.3} = +3.3V$ | | 0.025 | | A |
| I_{DDC} | 10BASE-T (Digital Core) | $V_{DD1.8} = +1.8V$ | | 0.234 | | A |
| Auto-Negotiation Mode: SDOCLK = 125MHz | | | | | | |
| I_{TX} | 10BASE-T (Analog TX) | $V_{DDA3.3} = +3.3V$ | | 0.032 | | A |
| I_{RX} | 10BASE-T (Analog RX) | $V_{DDA1.8} = +1.8V$ | | 0.07 | | A |
| I_{DDIO} | 10BASE-T (Digital I/O) | $V_{DD3.3} = +3.3V$ | | 0.021 | | A |
| I_{DDC} | 10BASE-T (Digital Core) | $V_{DD1.8} = +1.8V$ | | 0.233 | | A |
| TTL Inputs (PCI, LED, Memory Interface, UART) | | | | | | |
| V_{IH} | Input High Voltage | | 2.0 | | | V |
| V_{IL} | Input Low Voltage | | | | 0.8 | V |
| I_{IN} | Input Current (Excluding pull-up/pull-down) | $V_{IN} = GND \sim V_{DD3.3}$ | -10 | | 10 | μA |
| TTL Outputs (PCI, LED, Memory Interface, UART) | | | | | | |
| V_{OH} | Output High Voltage | $I_{OH} = -8mA; V_{DD3.3}$ | 2.4 | | | V |
| V_{OL} | Output Low Voltage | $I_{OL} = 8mA$ | | | 0.7 | V |
| I_{OZ} | Output Tri-state Leakage | | | | 10 | μA |

Notes:

- Exceeding the absolute maximum rating may damage the device.
- The device is not guaranteed to operate from either a 2.5V or 3.3V supply.
- V_{DDA} or V_{DD} can operate from either a 2.5V or 3.3V supply.
- No heat spreader in package.
- Specification for packaged product only.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|----------------------------------|---|------|-----|-----------|-------|
| 100BASE-TX Transmit (measured differentially after 1:1 transformer) | | | | | | |
| V_O | Peak Differential Output Voltage | 100 Ω termination on the differential output | 0.95 | | 1.05 | V |
| V_{IMB} | Output Voltage Imbalance | 100 Ω termination on the differential output | | | 2 | % |
| t_r t_f | Rise/Fall Time | | 3 | | 5 | ns |
| | Rise/Fall Time Imbalance | | 0 | | 0.5 | ns |
| | Duty Cycle Distortion | | | | ± 0.5 | ns |
| | Overshoot | | | | 5 | % |
| V_{SET} | Reference Voltage of ISET | | | 0.5 | | V |
| | Output Jitters | Peak-to-peak | | 0.7 | 1.4 | ns |
| 10BASE-T Receive | | | | | | |
| V_{SQ} | Squelch Threshold | 5MHz square wave | | 400 | | mV |
| 10BASE-T Transmit (measured differentially after 1:1 transformer) | | | | | | |
| V_P | Peak Differential Output Voltage | 100 Ω termination on the differential output | | 2.3 | | V |
| | Jitters Added | 100 Ω termination on the differential output | | | ± 3.5 | ns |
| | Rise/Fall Time | | | 28 | 30 | ns |

Timing Diagrams

For PCI timing, please refer to the PCI specification, version 2.1.

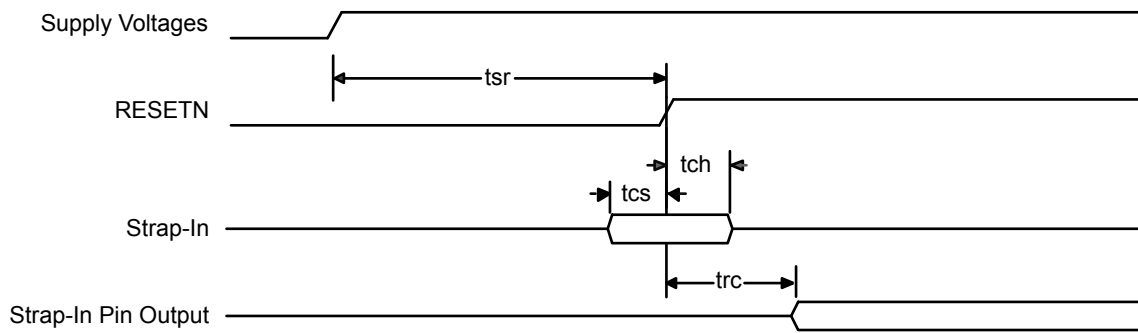


Figure 11. Reset Timing

| Symbol | Parameter | Min | Typ | Max | Units |
|----------|--------------------------------------|-----|-----|-----|-------|
| t_{SR} | Stable supply voltages to reset high | 10 | | | ms |
| t_{CS} | Configuration set-up time | 50 | | | ns |
| t_{CH} | Configuration hold time | 50 | | | ns |
| t_{RC} | Reset to strap-in pin output | 50 | | | ns |

Table 2. Reset Timing Parameters

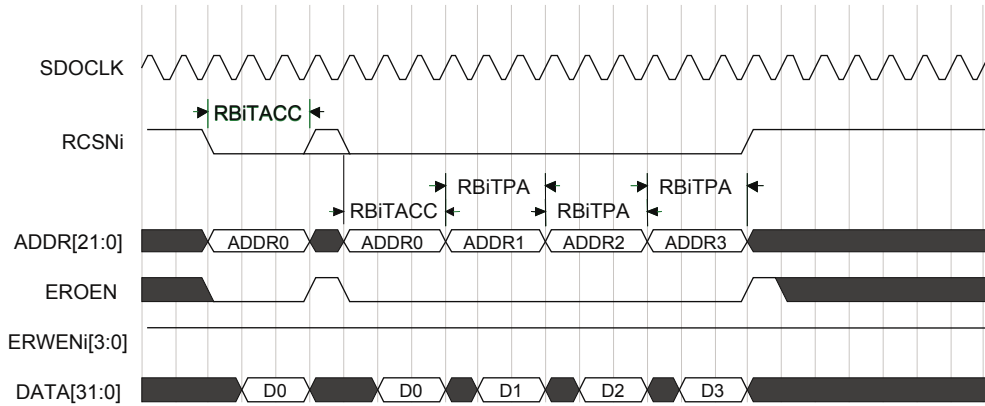


Figure 12. Static Memory Read Cycle

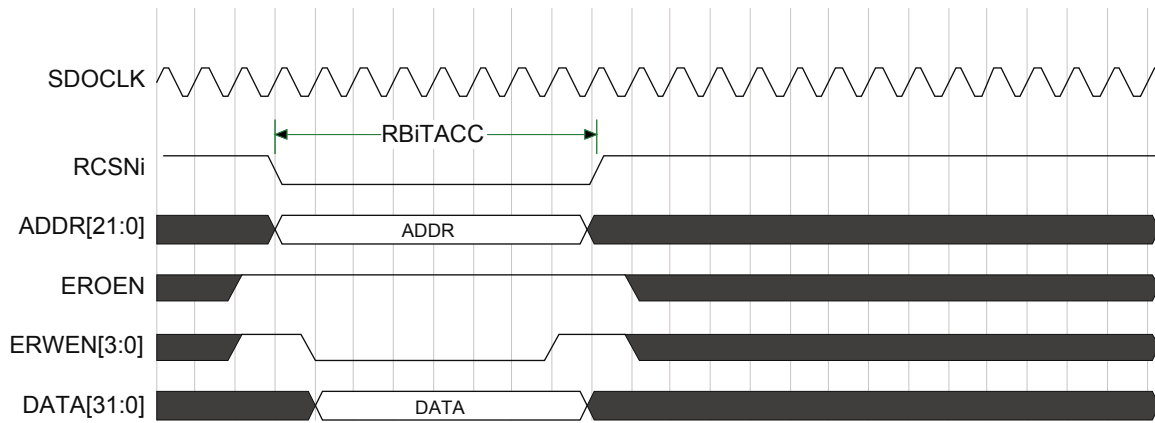


Figure 13. Static Memory Write Cycle

| Symbol | Parameter ⁽¹⁾ | Registers |
|---------|--------------------------------------|-----------|
| RBitACC | Programmable bank i access time | 0x4010 |
| RBitPA | Programmable bank i page access time | 0x4014 |

Table 3. Programmable Static Memory Timing Parameters

Note:

1. "i" Refers to chip select parameters 0 and 1.

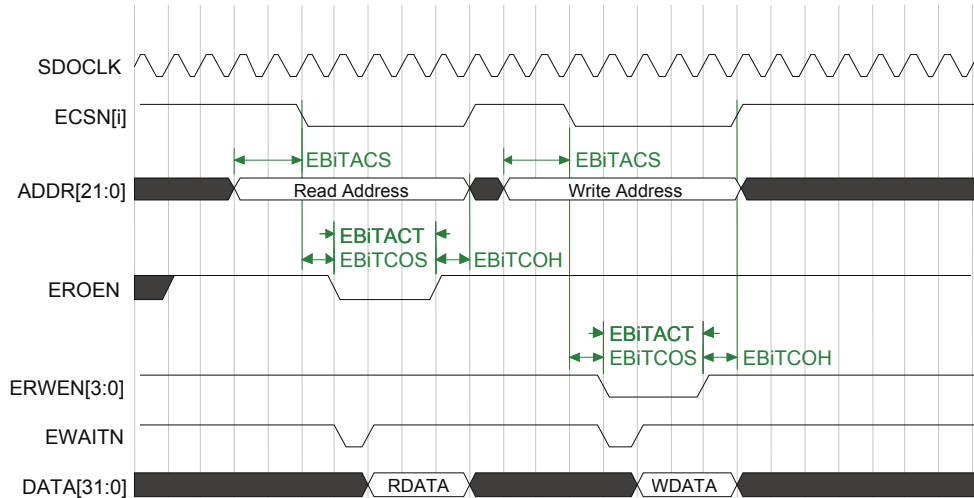


Figure 14. External I/O Read and Write Cycles

| Symbol | Parameter | Min ⁽¹⁾ | Typ ⁽¹⁾ | Max ⁽¹⁾ | Units |
|-------------------------------------|--|--------------------|--------------------|--------------------|-------|
| T _{cta} | Valid address to CS setup time +0.8 | EBiTACS +1.1 | EBiTACS +1.3 | EBiTACS ns | |
| T _{cos} | OE valid to CS setup time +0.6 | EBiTCOS +0.6 | EBiTCOS +1.0 | EBiTCOS ns | |
| T _{dsu} | Valid read data to OE setup time | 2.0 | | | ns |
| T _{cws} | WE valid to CS setup time +0.6 | EBiTCOS +0.6 | EBiTCOS +1.0 | EBiTCOS ns | |
| T _{dh} | Write data to CS hold time | 0 | | | ns |
| T _{cah} | Address to CS hold time +1.0 | EBiTCOH +1.0 | EBiTCOH +1.4 | EBiTCOH ns | |
| T _{oew} | OE/WE pulsewidth | EBiTACT | | EBiTACT | ns |
| T _{ocs} , T _{csw} | Rising edge CS to OE/WE hold time | 0 | | | ns |

Table 4. External I/O Memory Timing Parameters

Note:

1. Measurements for minimum were taken at 0°C, typical at 25°C, and maximum at 100°C.

| Symbol | Parameter ⁽¹⁾ | Registers |
|---------|--|------------------------|
| EBiTACS | Programmable bank i address setup time before chip select | 0x4000, 0x4004, 0x4008 |
| EBiTACT | Programmable bank i write enable/output enable access time | 0x4000, 0x4004, 0x4008 |
| EBiTCOS | Programmable bank i chip select setup time before OEN | 0x4000, 0x4004, 0x4008 |
| EBiTCOH | Programmable bank i chip select hold time | 0x4000, 0x4004, 0x4008 |

Table 5. Programmable External I/O Timing Parameters

Note:

1. "i" Refers to chip select parameters 0, 1, or 2.

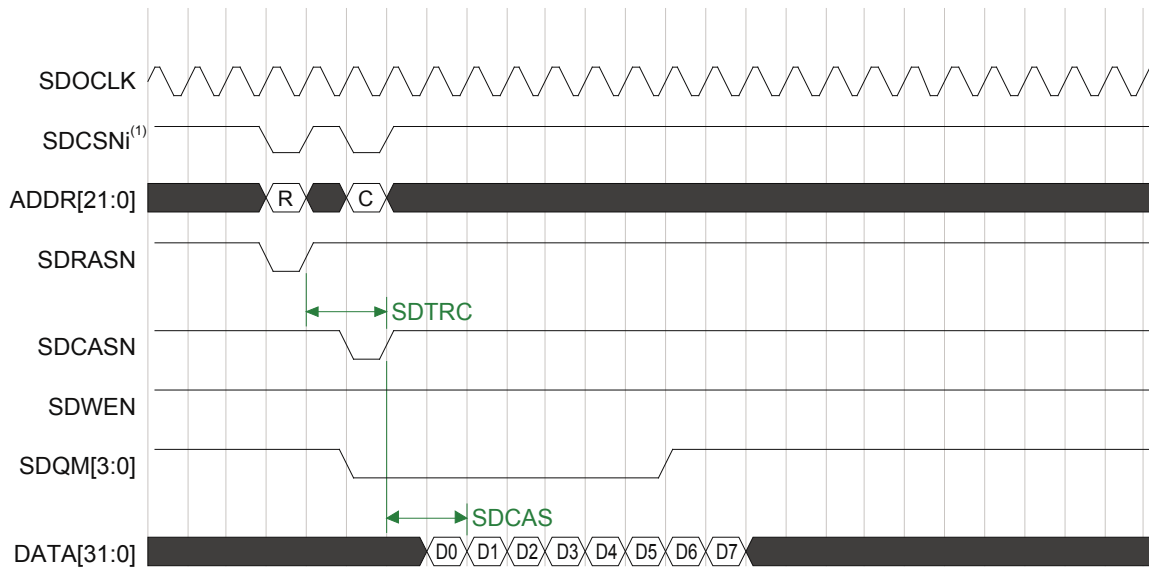


Figure 15. SDRAM Read Timing

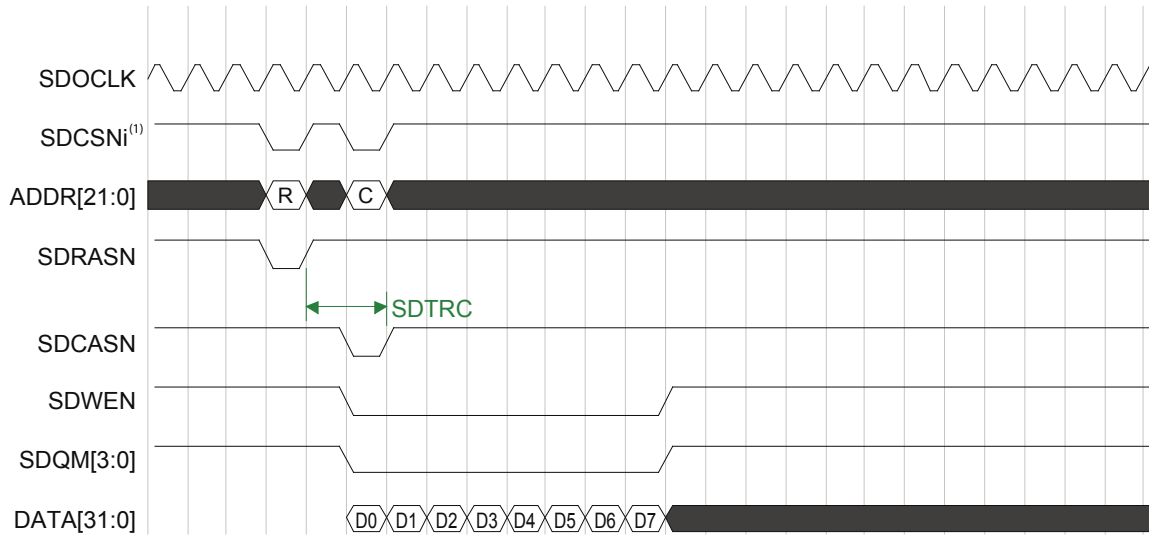


Figure 16. SDRAM Write Timing

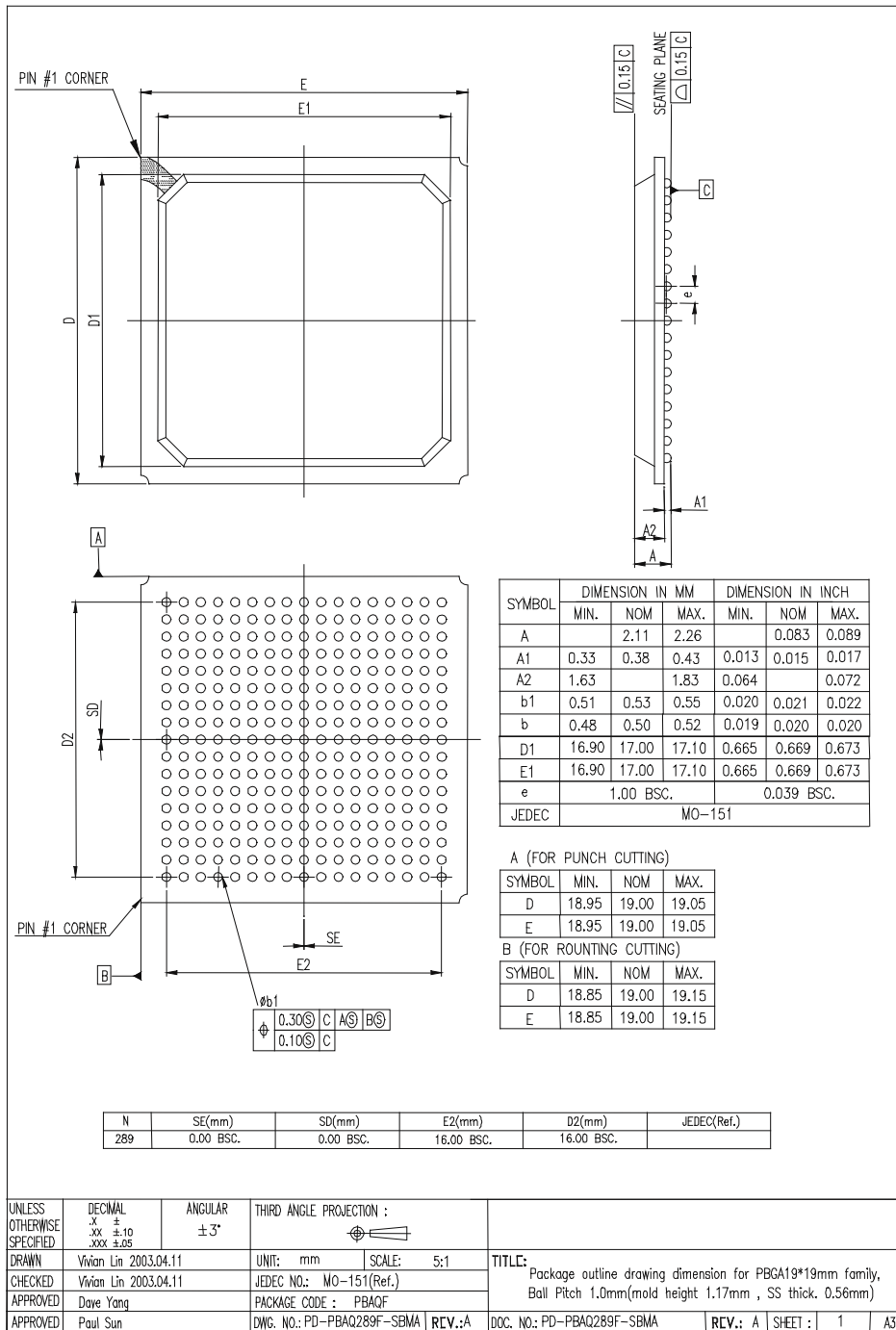
| Symbol | Parameter | Registers |
|--------|---------------------------------------|-----------|
| SDTRC | Programmable SDRAM RAS to CAS latency | 0x4038 |
| SDCAS | Programmable SDRAM CAS latency | 0x4038 |

Table 6. SDRAM Timing Parameters

Note:

- "i" refers to chip select parameters 0,1.

Package Information



289-Pin PBGA

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA

TEL + 1 (408) 944-0800 FAX + 1 (408) 474-1000 WEB <http://www.micrel.com>

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