DATA SHEET

Family Specifications

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Philips
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Family Specifications

INTRODUCTION

These specifications cover the common electrical characteristics of the entire HE4000B family, unless otherwise specified in the individual device data sheet.

The LOCMOS HE4000B family devices will operate over a recommended V_{DD} power supply range of 3 to 15 V, as referenced to V_{SS} (usually ground). Parametric limits are guaranteed for V_{DD} of 5, 10 and 15 V. Because of the wide operating voltage, power supply regulation is less critical than with other types of logic. The lower limit of the supply voltage is 3 V, or as determined by required system speed and/or noise immunity or interface to other logic. The recommended upper limit is 15 V or as determined by power dissipation constraints or interface to other logic. Unused inputs must be connected to V_{DD}, V_{SS} or another input. Inputs and outputs are protected against electrostatic effects in a wide variety of device-handling situations. However, to be totally safe, it is desirable to take handling precautions into account.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply voltage		–0.5	–	+18	V
V_I	Voltage on any input		–0.5	–	V_{DD} + 0.5	V
±I	DC current into any input or output		–	–	10	mA
P_{tot}	Power dissipation per package					
	HEF (plastic and ceramic DIL)	T_{amb} = –40 to +70 °C			750	mW
		T_{amb} = +70 to +85 °C	derate linearly with 12 mW/K			
	HEF (plastic SO mini-pack)	T_{amb} = –40 to +70 °C			500	mW
		T_{amb} = +70 to +85 °C	derate linearly with 8 mW/K			
	HEC (ceramic DIL)	T_{amb} = –55 to +70 °C			500	mW
		T_{amb} = +70 to +125 °C	derate linearly with 8 mW/K			
P	Power dissipation per output		–	–	100	mW
T_{stg}	Storage temperature		–65	–	+150	°C
T_{amb}	Operating ambient temperature (HEF)		–40	–	+85	°C
T_{amb}	Operating ambient temperature (HEC)		–55	–	+125	°C

DC CHARACTERISTICS FOR HEF

V_{SS} = 0 V; for all devices unless otherwise specified.

SYMBOL	PARAMETER	V_{DD} (V)	T_{amb} (°C)						UNIT	CONDITIONS
			−40		+25		+85			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
I_{DD}	Quiescent device current									
	gates	5	–	1.0	–	1.0	–	7.5	µA	all valid input combinations; $V_I = V_{SS}$ or V_{DD}; $I_O = 0$
		10	–	2.0	–	2.0	–	15.0		
		15	–	4.0	–	4.0	–	30.0		
	buffers, flip-flops	5	–	4.0	–	4.0	–	30	µA	
		10	–	8.0	–	8.0	–	60		
		15	–	16.0	–	16.0	–	120		
	MSI	5	–	20	–	20	–	150	µA	
		10	–	40	–	40	–	300		
		15	–	80	–	80	–	600		
	LSI	5	–	50	–	50	–	375	µA	
		10	–	100	–	100	–	750		
		15	–	200	–	200	–	1500		
V_{OL}	Output voltage LOW	5	–	0.05	–	0.05	–	0.05	V	$V_I = V_{SS}$ or V_{DD}; $\|I_O\| < 1$ µA
		10	–	0.05	–	0.05	–	0.05		
		15	–	0.05	–	0.05	–	0.05		
V_{OH}	Output voltage HIGH	5	4.95	–	4.95	–	4.95	–	V	$V_I = V_{SS}$ or V_{DD}; $\|I_O\| < 1$ µA
		10	9.95	–	9.95	–	9.95	–		
		15	14.95	–	14.95	–	14.95	–		
V_{IL}	Input voltage LOW (buffered stages only)	5	–	1.5	–	1.5	–	1.5	V	V_O = 0.5 V or 4.5 V; $\|I_O\| < 1$ µA
		10	–	3.0	–	3.0	–	3.0		V_O = 1.0 V or 9.0 V; $\|I_O\| < 1$ µA
		15	–	4.0	–	4.0	–	4.0		V_O = 1.5 V or 13.5 V; $\|I_O\| < 1$ µA
V_{IH}	Input voltage HIGH (buffered stages only)	5	3.5	–	3.5	–	3.5	–	V	V_O = 0.5 V or 4.5 V; $\|I_O\| < 1$ µA
		10	7.0	–	7.0	–	7.0	–		V_O = 1.0 V or 9.0 V; $\|I_O\| < 1$ µA
		15	11.0	–	11.0	–	11.0	–		V_O = 1.5 V or 13.5 V; $\|I_O\| < 1$ µA

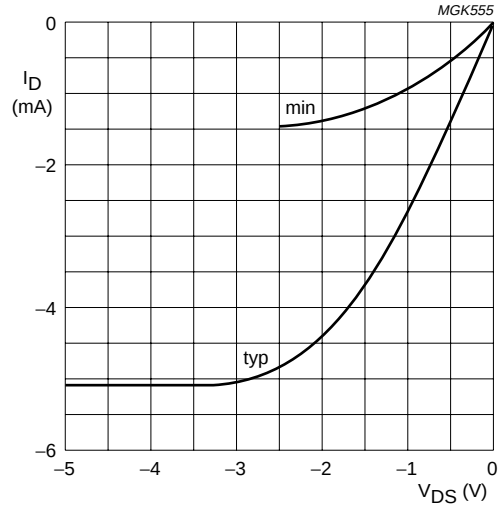
SYMBOL	PARAMETER	V_{DD} (V)	T_{amb} (°C)						UNIT	CONDITIONS
			−40		+25		+85			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
V_{IL}	Input voltage LOW (unbuffered stages only)	5	–	1	–	1	–	1	V	V_O = 0.5 V or 4.5 V; $\|I_O\|$ < 1 μA
		10	–	2	–	2	–	2		V_O = 1.0 V or 9.0 V; $\|I_O\|$ < 1 μA
		15	–	2.5	–	2.5	–	2.5		V_O = 1.5 V or 13.5 V; $\|I_O\|$ < 1 μA
V_{IH}	Input voltage HIGH (unbuffered stages only)	5	4	–	4	–	4	–	V	V_O = 0.5 V or 4.5 V; $\|I_O\|$ < 1 μA
		10	8	–	8	–	8	–		V_O = 1.0 V or 9.0 V; $\|I_O\|$ < 1 μA
		15	12.5	–	12.5	–	12.5	–		V_O = 1.5 V or 13.5 V; $\|I_O\|$ < 1 μA
I_{OL}	Output (sink) current LOW	5	0.52	–	0.44	–	0.36	–	mA	V_O = 0.4 V; V_I = 0 or 5 V
		10	1.3	–	1.1	–	0.9	–		V_O = 0.5 V; V_I = 0 or 10 V
		15	3.6	–	3.0	–	2.4	–		V_O = 1.5 V; V_I = 0 or 15 V
$-I_{OH}$	Output (source) current HIGH	5	0.52	–	0.44	–	0.36	–	mA	V_O = 4.6 V; V_I = 0 or 5 V
		10	1.3	–	1.1	–	0.9	–		V_O = 9.5 V; V_I = 0 or 10 V
		15	3.6	–	3.0	–	2.4	–		V_O = 13.5 V; V_I = 0 or 15 V
$-I_{OH}$	Output (source) current HIGH	5	1.7	–	1.4	–	1.1	–	mA	V_O = 2.5 V; V_I = 0 or 5 V
± I_{IN}	Input leakage current	15	–	0.3	–	0.3	–	1.0	μA	V_I = 0 or 15 V
I_{OZH}	3-state output leakage current; HIGH	15	–	1.6	–	1.6	–	12.0	μA	output returned to V_{DD}
$-I_{OZL}$	3-state output leakage current; LOW	15	–	1.6	–	1.6	–	12.0	μA	output returned to V_{SS}

DC CHARACTERISTICS FOR HEC

V_{SS} = 0 V; for all devices unless otherwise specified.

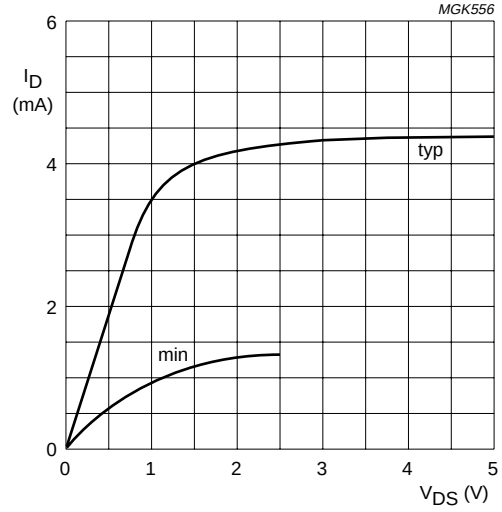
SYMBOL	PARAMETER	V_{DD} (V)	T_{amb} (°C)						UNIT	CONDITIONS
			−55		+25		+125			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
I_{DD}	Quiescent device current									
	gates	5	–	0.25	–	0.25	–	7.5	µA	all valid input combinations; $V_I = V_{SS}$ or V_{DD}; $I_O = 0$
		10	–	0.5	–	0.5	–	15.0		
		15	–	1.0	–	1.0	–	30.0		
	buffers, flip-flops	5	–	1.0	–	1.0	–	30	µA	
		10	–	2.0	–	2.0	–	60		
		15	–	4.0	–	4.0	–	120		
	MSI	5	–	5.0	–	5.0	–	150	µA	
		10	–	10.0	–	10.0	–	300		
		15	–	20.0	–	20.0	–	600		
	LSI	5	–	15	–	15	–	375	µA	
		10	–	25	–	25	–	750		
		15	–	50	–	50	–	1500		
V_{OL}	Output voltage LOW	5	–	0.05	–	0.05	–	0.05	V	$V_I = V_{SS}$ or V_{DD}; $\lvert I_O \rvert < 1$ µA
		10	–	0.05	–	0.05	–	0.05		
		15	–	0.05	–	0.05	–	0.05		
V_{OH}	Output voltage HIGH	5	4.95	–	4.95	–	4.95	–	V	$V_I = V_{SS}$ or V_{DD}; $\lvert I_O \rvert < 1$ µA
		10	9.95	–	9.95	–	9.95	–		
		15	14.95	–	14.95	–	14.95	–		
V_{IL}	Input voltage LOW (buffered stages only)	5	–	1.5	–	1.5	–	1.5	V	V_O = 0.5 V or 4.5 V; $\lvert I_O \rvert < 1$ µA
		10	–	3.0	–	3.0	–	3.0		V_O = 1.0 V or 9.0 V; $\lvert I_O \rvert < 1$ µA
		15	–	4.0	–	4.0	–	4.0		V_O = 1.5 V or 13.5 V; $\lvert I_O \rvert < 1$ µA
V_{IH}	Input voltage HIGH (buffered stages only)	5	3.5	–	3.5	–	3.5	–	V	V_O = 0.5 V or 4.5 V; $\lvert I_O \rvert < 1$ µA
		10	7.0	–	7.0	–	7.0	–		V_O = 1.0 V or 9.0 V; $\lvert I_O \rvert < 1$ µA
		15	11.0	–	11.0	–	11.0	–		V_O = 1.5 V or 13.5 V; $\lvert I_O \rvert < 1$ µA

SYMBOL	PARAMETER	V_{DD} (V)	T_{amb} (°C)						UNIT	CONDITIONS
			−55		+25		+125			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
V_{IL}	Input voltage LOW (unbuffered stages only)	5	–	1	–	1	–	1	V	V_O = 0.5 V or 4.5 V; $\|I_O\|$ < 1 μA
		10	–	2	–	2	–	2		V_O = 1.0 V or 9.0 V; $\|I_O\|$ < 1 μA
		15	–	2.5	–	2.5	–	2.5		V_O = 1.5 V or 13.5 V; $\|I_O\|$ < 1 μA
V_{IH}	Input voltage HIGH (unbuffered stages only)	5	4	–	4	–	4	–	V	V_O = 0.5 V or 4.5 V; $\|I_O\|$ < 1 μA
		10	8	–	8	–	8	–		V_O = 1.0 V or 9.0 V; $\|I_O\|$ < 1 μA
		15	12.5	–	12.5	–	12.5	–		V_O = 1.5 V or 13.5 V; $\|I_O\|$ < 1 μA
I_{OL}	Output (sink) current LOW	5	0.64	–	0.5	–	0.36	–	mA	V_O = 0.4 V; V_I = 0 or 5 V
		10	1.6	–	1.3	–	0.9	–		V_O = 0.5 V; V_I = 0 or 10 V
		15	4.2	–	3.4	–	2.4	–		V_O = 1.5 V; V_I = 0 or 15 V
$-I_{OH}$	Output (source) current HIGH	5	0.64	–	0.5	–	0.36	–	mA	V_O = 4.6 V; V_I = 0 or 5 V
		10	1.6	–	1.3	–	0.9	–		V_O = 9.5 V; V_I = 0 or 10 V
		15	4.2	–	3.4	–	2.4	–		V_O = 13.5 V; V_I = 0 or 15 V
$-I_{OH}$	Output (source) current HIGH	5	1.7	–	1.4	–	1.1	–	mA	V_O = 2.5 V; V_I = 0 or 5 V
± I_{IN}	Input leakage current	15	–	0.1	–	0.1	–	1.0	μA	V_I = 0 or 15 V
I_{OZH}	3-state output leakage current; HIGH	15	–	0.4	–	0.4	–	12.0	μA	output returned to V_{DD}
$-I_{OZL}$	3-state output leakage current; LOW	15	–	0.4	–	0.4	–	12.0	μA	output returned to V_{SS}



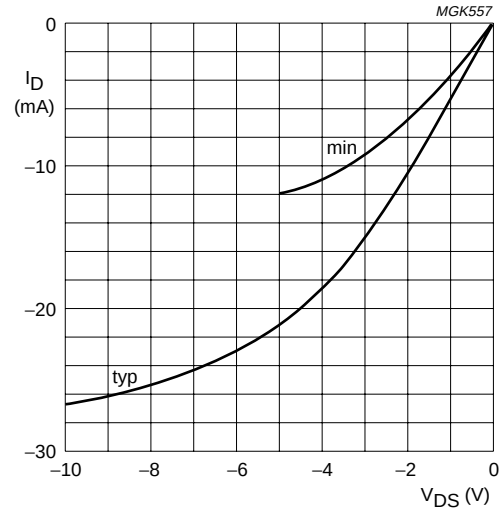
V_{DD} = 5 V; T_{amb} = 25 °C

Fig.1 P-channel drain characteristics (source).



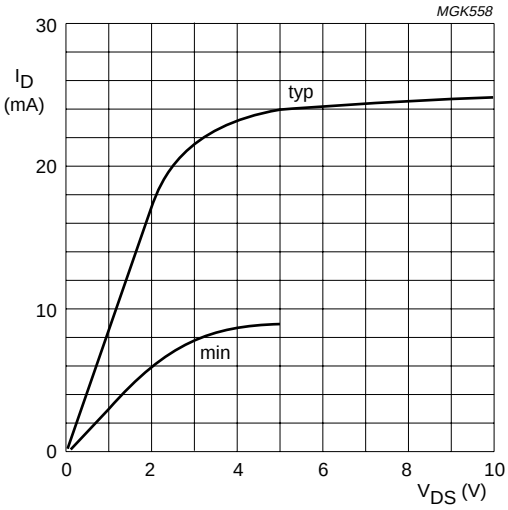
V_{DD} = 5 V; T_{amb} = 25 °C

Fig.2 N-channel drain characteristics (sink).



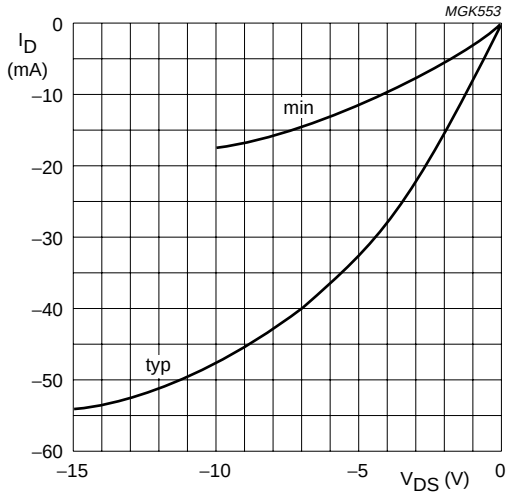
V_{DD} = 10 V; T_{amb} = 25 °C

Fig.3 P-channel drain characteristics (source).



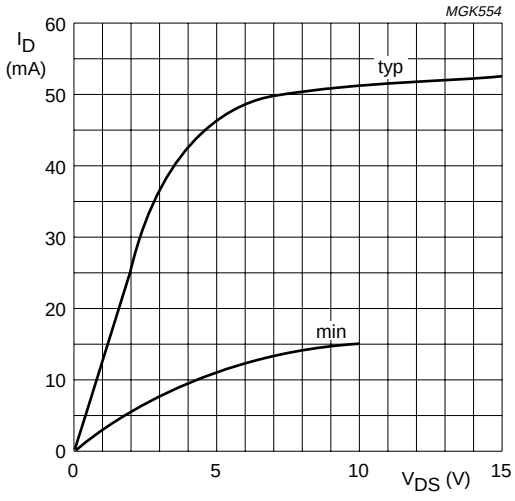
V_{DD} = 10 V; T_{amb} = 25 °C

Fig.4 N-channel drain characteristics (sink).



V_{DD} = 15 V; T_{amb} = 25 °C

Fig.5 P-channel drain characteristics (source).



V_{DD} = 15 V; T_{amb} = 25 °C

Fig.6 N-channel drain characteristics (sink).

Note: temperature coefficient: −0.4%/°C

AC CHARACTERISTICS

Clock input rise and fall times (t_r, t_f)

The upper limits on t_r and t_f vary widely from device to device and with supply voltage. Unless otherwise specified in the individual data sheets it is recommended that input rise and fall times be less than 15 μs for V_{DD} = 5 V; 4 μs for V_{DD} = 10 V; 1 μs for V_{DD} = 15 V.

Output transition times (t_{TLH}, t_{THL})

V_{SS} = 0; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns.

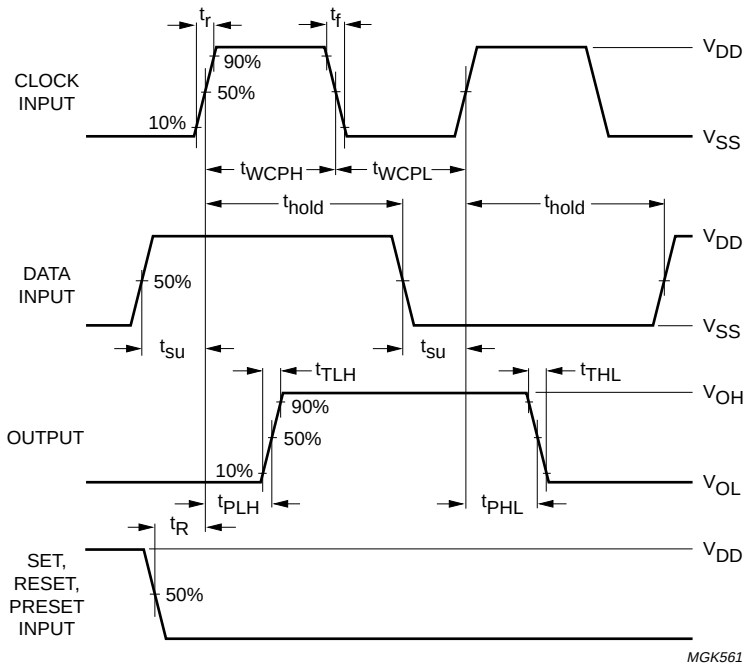
SYMBOL	PARAMETER	V_{DD} (V)	MIN.	TYP.	MAX.	UNIT	TYPICAL EXTRAPOLATION FORMULA
	output transition times						
t_{THL}	HIGH to LOW	5		60	120	ns	10 ns + (1.0 ns/pF) C_L
		10		30	60	ns	9 ns + (0.42 ns/pF) C_L
		15		20	40	ns	6 ns + (0.28 ns/pF) C_L
t_{TLH}	LOW to HIGH	5		60	120	ns	10 ns + (1.0 ns/pF) C_L
		10		30	60	ns	9 ns + (0.42 ns/pF) C_L
		15		20	40	ns	6 ns + (0.28 ns/pF) C_L

Temperature coefficient (typical values)

Propagation delays	+0.35%/°C
Output transition times	+0.35%/°C

Input capacitance (digital inputs)

Maximum input capacitance C_I = 7.5 pF



In the waveforms above the active transition of the clock input is going from LOW to HIGH and the active level of the forcing signals (SET, CLEAR and PRESET) is HIGH.

The actual direction of the active transition of the clock input and the actual active levels of the forcing signals are specified in the individual device data sheet.

Fig.7 Set-up times, hold times, recovery times and propagation delays for sequential logic circuits.

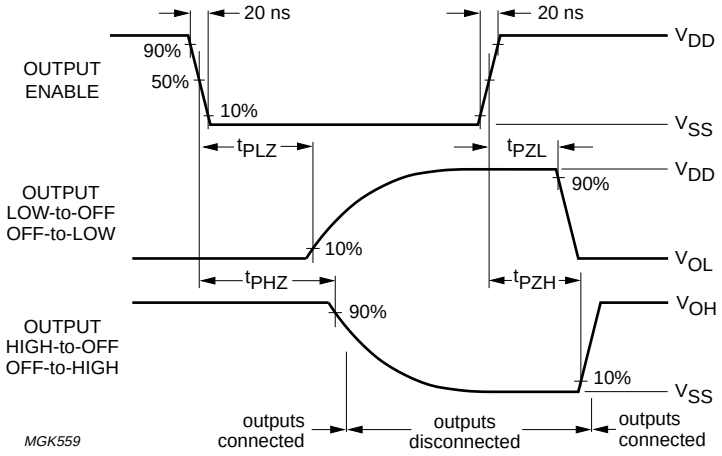


Fig.8 Propagation delays of 3-state outputs.

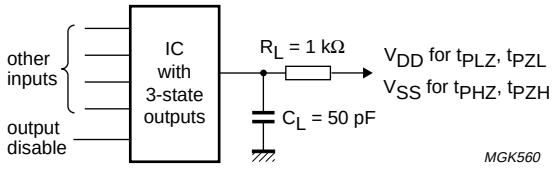


Fig.9 Test circuit of 3-state output ICs.

DEFINITIONS OF SYMBOLS AND TERMS USED IN DATA SHEETS

Currents

Positive current is defined as conventional current flow into a device.
Negative current is defined as conventional current flow out of a device.

I_{IN}	Input current; the current flowing into a device at specified input voltage and V_{DD}.
I_{OH}	Output current HIGH; the drive current flowing out of a device at specified HIGH output voltage and V_{DD}.
I_{OL}	Output current LOW; the drive current flowing into a device at specified LOW output voltage and V_{DD}.
I_{DD}	Quiescent power supply current; the current flowing into the V_{DD} lead at specified input and V_{DD} conditions.
I_{OZ}	Output OFF current; the leakage current flowing into or out of the output of a 3-state device in the OFF state when the output is connected to V_{DD} or V_{SS}.
I_{IL}	Input current LOW; the current flowing into a device at a specified LOW level input voltage and a specified V_{DD}.
I_{IH}	Input current HIGH; the current flowing into a device at a specified HIGH level input voltage and a specified V_{DD}.
I_{DDL}	Quiescent power supply current LOW; the current flowing into the V_{DD} lead with a specified LOW level input voltage on all inputs and specified V_{DD} conditions.
I_{DDH}	Quiescent power supply current HIGH; the current flowing into the V_{DD} lead with a specified HIGH level input voltage on all inputs and specified V_{DD} conditions.
I_Z	OFF state leakage current; the leakage current flowing into the output of a 3-state device in the OFF state at a specified output voltage and V_{DD}.

Voltages

All voltages are referenced to V_{SS}, which is the most negative potential applied to the device.

V_{DD}	Supply voltage; the most positive potential on the device.
V_{SS}	Supply voltage; for a device with a single negative power supply, the most negative power supply, used as the reference level for other voltages; typically ground.
V_{EE}	Supply voltage; one of two (V_{SS} and V_{EE}) negative power supplies. For a device with dual negative power supply, the most negative power supply as a reference level for other voltages.
V_{IH}	Input voltage HIGH; the range of input voltages that represents a logic HIGH level in the system.
V_{IL}	Input voltage LOW; the range of input voltages that represents a logic LOW level in the system.
V_{OH}	Output voltage HIGH; the range of voltages at an output terminal with a specified output loading and supply voltage. Device inputs are conditioned to establish a HIGH level at the output.
V_{OL}	Output voltage LOW; the range of voltages at an output terminal with a specified output loading and supply voltage. Device inputs are conditioned to establish a LOW level at the output.
V_P	Trigger threshold voltage; positive-going signal.
V_N	Trigger threshold voltage; negative-going signal.

Analogue terms

R_{ON}	ON resistance; the effective ON state resistance of an analogue transmission gate, at specified input voltage, output load and V_{DD}.
ΔR_{ON}	ΔON resistance; the difference in effective ON resistance between any two transmission gates of an analogue device at specified input voltage, output load and V_{DD}.

AC switching parameters

f_i Input frequency; for combinatorial logic devices the maximum number of inputs and outputs switching in accordance with the device truth table. For sequential logic devices the clock frequency using alternate HIGH and LOW for data input or using the toggle mode, whichever is applicable.

f_o Output frequency; each output.

f_{max} Clock frequency; clock input waveform should have a 50% duty cycle and be such as to cause the outputs to be switching from 10%V_{DD} to 90%V_{DD} in accordance with the device truth table.

t_r, t_f Clock input rise and fall times; 10% and 90% value.

t_{PLH} Propagation delay time; the time between the specified reference points, normally the 50% points on the input and output waveforms, with the output changing from the defined LOW level to the defined HIGH level.

t_{PHL} Propagation delay time; the time between the specified reference points, normally the 50% points on the input and output waveforms, with the output changing from the defined HIGH level to the defined LOW level.

t_{TLH} Transition time, LOW-to-HIGH; the time between two specified reference points on a waveform, normally 10% and 90% points, that is changing from LOW to HIGH.

t_{THL} Transition time, HIGH-to-LOW; the time between two specified reference points on a waveform, normally 90% and 10% points, that is changing from HIGH to LOW.

t_W Pulse width; the time between the 50% amplitude points on the leading and trailing edges of a pulse.

t_{hold} Hold time; the interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure their continued recognition. A negative hold time indicates that the correct logic level may be released prior to the timing pulse and still be recognized.

t_{su} Set-up time; the interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure their recognition. A negative set-up time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.

t_{PHZ} 3-state output disable time, HIGH to Z; the time between the specified reference points, normally the 50% point on the output enable input voltage waveform and a point representing a 0.1 V_{OH} drop on the output voltage waveform of a 3-state device, with the output changing from the output HIGH level (V_{OH}) to a high impedance OFF-state.

t_{PLZ} 3-state output disable time, LOW to Z; the time between the specified reference points, normally the 50% point on the output enable input voltage waveform and a point representing a 0.1 (V_{DD} – V_{OL}) rise on the output voltage waveform of a 3-state device, with the output changing from the output LOW level (V_{OL}) to a high impedance OFF-state.

t_{PZH} 3-state output enable time, Z to HIGH; the time between the specified reference points, normally the 50% point on the output enable input voltage waveform and a point representing a 0.1 V_{OH} rise on the output voltage waveform of a 3-state device, with the output changing from a high impedance OFF-state to the output HIGH level (V_{OH}).

t_{PZL} 3-state output enable time, Z to LOW; the time between the specified reference points, normally the 50% point on the output enable input voltage waveform and a point representing a 0.1 (V_{DD} – V_{OL}) voltage drop on the output voltage waveform of a 3-state device, with the output changing from a high impedance OFF-state to the output LOW level (V_{OL}).

t_R Recovery time; the time between the end of an overriding asynchronous input, typically a clear or reset input, and the earliest permissible beginning of a synchronous control input, typically a clock input, normally measured at 50% points on both input voltage waveforms.