2SK2988

Silicon N-Channel Junction FET

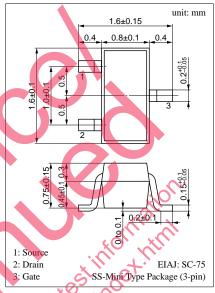
For impedance conversion in low frequency For pyroelectric sensor

■ Features

- Low noise-figure (NF)
- High gate to drain voltage V_{GDO}
- SS-mini type package, allowing downsizing of the sets and automatic insertion through the tape/magazine packing.

■ Absolute Maximum Ratings (Ta = 25 ± 3°C

Parameter	Symbol	Ratings	Unit	
Gate to Drain voltage	V _{GDS}	-40	V	
Drain current	I_{D}	10	mA	
Gate current	I_{G}	2	mA	
Allowable power dissipation	P_{D}	125	mW	
Channel temperature	T _{ch}	125	°C	
Storage temperature	T _{stg}	-55 to +150	°C	



	Symbol	Ratings	Unit		, ,	9///	11.
Gate to Drain voltage	V _{GDS}	-40	V	1: Source	10:		•
Drain current	I_{D}	10	mA	2: Drain 3: Gate	SS-M	E ini Type Pack	IAJ: SC-75 age (3-pin)
Gate current	I_{G}	2	mA			3	
Allowable power dissipation	P_{D}	125	mW	Marking S	ymbol:	HS	
Channel temperature	T _{ch}	125	°C	Oll C	$U_{I_{\alpha}}$		
Storage temperature	T _{stg}	-55 to +150	°C	20,00)		
■ Electrical Characterist	iCS (Ta =	110	mA mW °C °C	min	typ	max	
		A			71		Unit
Drain to Source cut-off current	Ines	$V_{DS} = 10V$, V_{CS}	≥ 0	1.4		4.7	Unit
Drain to Source cut-off current Gate to Source leakage current	I_{DSS} I_{GSS}	$V_{DS} = 10V, V_{GS}$ $V_{GS} = -20V, V_{DS}$		1.4			
	I _{GSS}	13 41.	$_{S}=0$	1.4 -40		4.7	mA
Gate to Source leakage current	•	$V_{GS} = -20V_{O}V_{D}$	S = 0 $OS = 0$			4.7	mA nA
Gate to Source leakage current Gate to Drain voltage	I _{GSS}	$V_{GS} = -20V_{o}V_{D}$ $I_{G} = -100\mu A, V_{I}$	$S = 0$ $DS = 0$ $1\mu A$			4.7	mA nA V
Gate to Source leakage current Gate to Drain voltage Gate to Source cut-off voltage	I _{GSS} V _{GDS} V _{GSQ}	$V_{OS} = -20V, V_{D}$ $I_{G} = -100\mu A, V_{I}$ $V_{DS} = 10V, I_{D} =$	$S = 0$ $DS = 0$ $1\mu A$	-40	5	4.7	mA nA V
Gate to Source leakage current Gate to Drain voltage Gate to Source cut-off voltage Forward transfer admittance	I _{GSS} V _{GDS} V _{GSO} Y _{fs}	$V_{OS} = -20V, V_{D}$ $I_{G} = -100\mu A, V_{I}$ $V_{DS} = 10V, I_{D} =$	S = 0 DS = 0 DA =	-40	5 1	4.7	mA nA V V mS

Note: The test method to comply with JISC7030, Field effect transistor test method.

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