SONET/SDH/ATM OC-48 DIFFERENTIAL 1:16 RECEIVER S3064

FEATURES

- Micro-power Bipolar technology
- Complies with Bellcore and ITU-T specifications
- Supports 2.488 Gbps (OC-48)
- Interface to both LVPECL and TTL logic
- 16-bit Differential LVPECL data path
- Compact 100 TQFP/TEP package
- Diagnostic loopback mode
- Line loopback
- Signal detect input
- Low jitter LVPECL interface
- Single 3.3V supply
- Typical Power 990 mW

APPLICATIONS

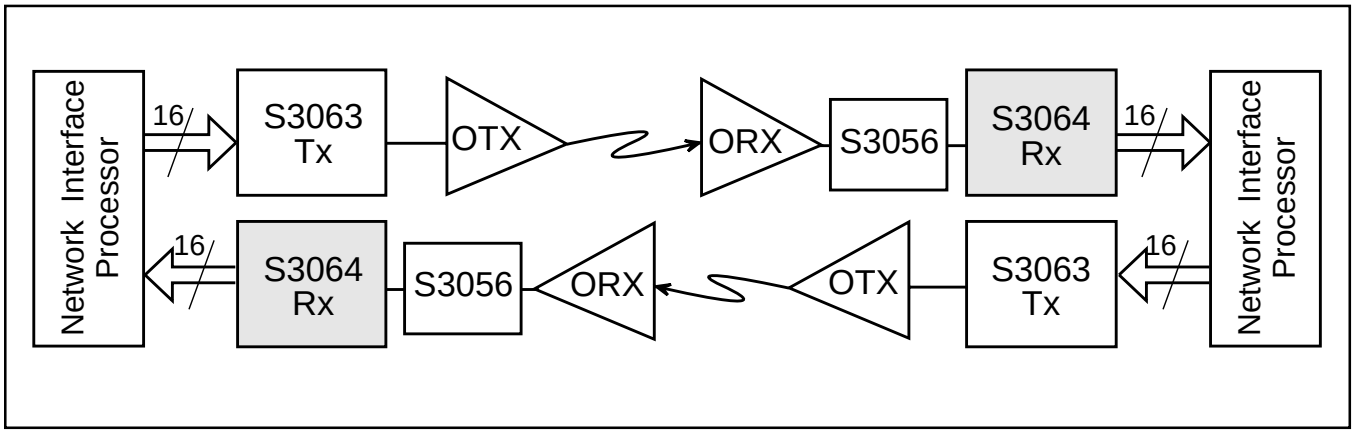
- SONET/SDH-based transmission systems
- SONET/SDH modules
- SONET/SDH test equipment
- ATM over SONET/SDH
- Section repeaters
- Add Drop Multiplexers (ADM)
- Broad-band cross-connects
- Fiber optic terminators
- Fiber optic test equipment

GENERAL DESCRIPTION

The S3064 SONET/SDH DeMUX chip is a fully integrated deserialization SONET OC-48 (2.488 Gbps) interface device. The chip performs all necessary serial-to-parallel and framing functions in conformance with SONET/SDH transmission standards. The device is suitable for SONET-based ATM applications. Figure 1 shows a typical network application.

The low jitter LVPECL interface guarantees compliance with the bit-error rate requirements of the Bellcore and ITU-T standards. The S3064 is packaged in a 100 TQFP/TEP, offering designers a small package outline.

Figure 1. System Block Diagram



SONET OVERVIEW

Synchronous Optical Network (SONET) is a standard for connecting one fiber system to another at the optical level. SONET, together with the Synchronous Digital Hierarchy (SDH) administered by the ITU-T, forms a single international standard for fiber interconnect between telephone networks of different countries. SONET is capable of accommodating a variety of transmission rates and applications.

The SONET standard is a layered protocol with four separate layers defined. These are:

- Photonic
- Section
- Line
- Path

Figure 2 shows the layers and their functions. Each of the layers has overhead bandwidth dedicated to administration and maintenance. The photonic layer simply handles the conversion from electrical to optical and back with no overhead. It is responsible for transmitting the electrical signals in optical form over the physical media. The section layer handles the transport of the framed electrical signals across the optical cable from one end to the next. Key functions of this layer are framing, scrambling, and error monitoring. The line layer is responsible for the reliable transmission of the path layer information stream carrying voice, data, and video signals. Its main functions are synchronization, multiplexing, and reliable transport. The path layer is responsible for the actual transport of services at the appropriate signaling rates.

Data Rates and Signal Hierarchy

Table 1 contains the data rates and signal designations of the SONET hierarchy. The lowest level is the basic SONET signal referred to as the synchronous transport signal level-1 (STS-1). An STS-*N* signal is made up of *N* byte-interleaved STS-1 signals. The optical counterpart of each STS-*N* signal is an optical carrier level-*N* signal (OC-*N*). The S3064 chip supports the OC-48 data rate (2.488 Gbps).

Frame and Byte Boundary Detection

The SONET/SDH fundamental frame format for STS-48 consists of 144 transport overhead bytes followed by Synchronous Payload Envelope (SPE) bytes. This pattern of 144 overhead and 4176 SPE bytes is repeated nine times in each frame. Frame and byte boundaries are detected using the A1 and A2 bytes found in the transport overhead. (See Figure 3.)

For more details on SONET operations, refer to the Bellcore SONET standard document.

Figure 2. SONET Structure

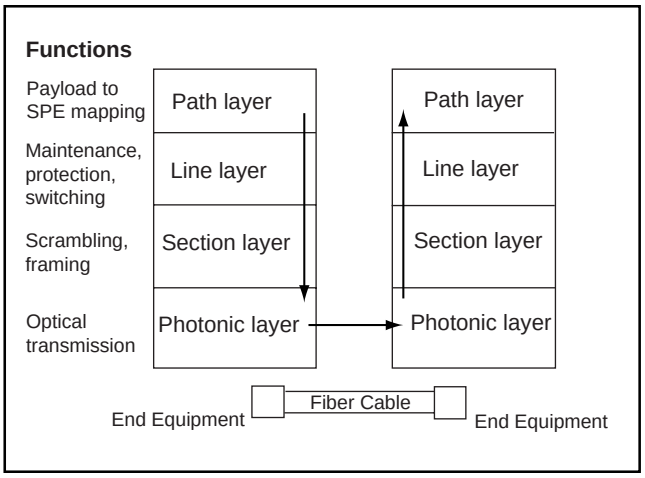
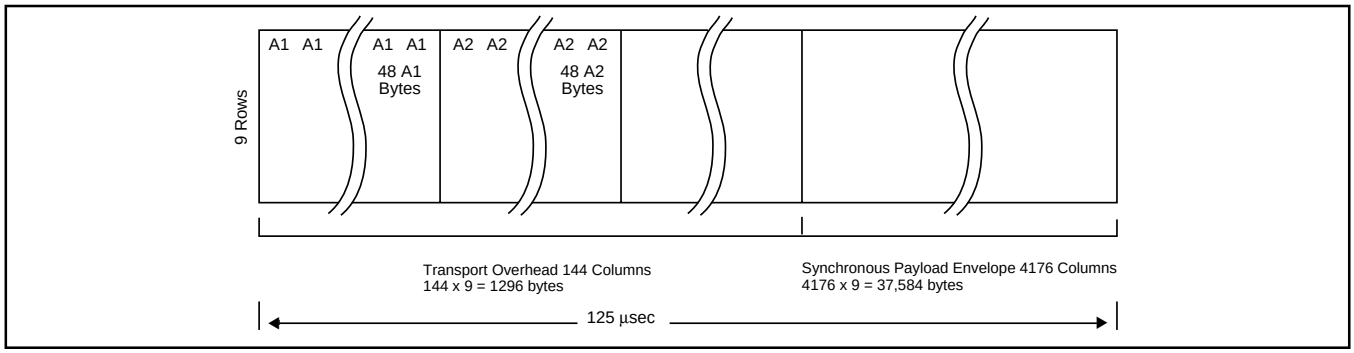


Table 1. SONET Signal Hierarchy

Elec.	CCITT	Optical	Data Rate (Mbps)
STS-1		OC-1	51.84
STS-3	STM-1	OC-3	155.52
STS-12	STM-4	OC-12	622.08
STS-24	STM-8	OC-24	1244.16
STS-48	STM-16	OC-48	2488.32

Figure 3. STS-48/OC-48 Frame Format



S3064 OVERVIEW

The S3064 receiver implements SONET/SDH deserialization and frame detection functions. The block diagram in Figure 4 shows the basic operation of the chip. This chip can be used to implement the front end of SONET equipment, which consists primarily of the serial transmit interface and the serial receive interface. The chip includes serial-to-parallel conversion and system timing. The system timing circuitry consists of management of the datastream, framing, and clock distribution throughout the front end.

The sequence of operations of the S3064 is as follows:

Receiver Operations:

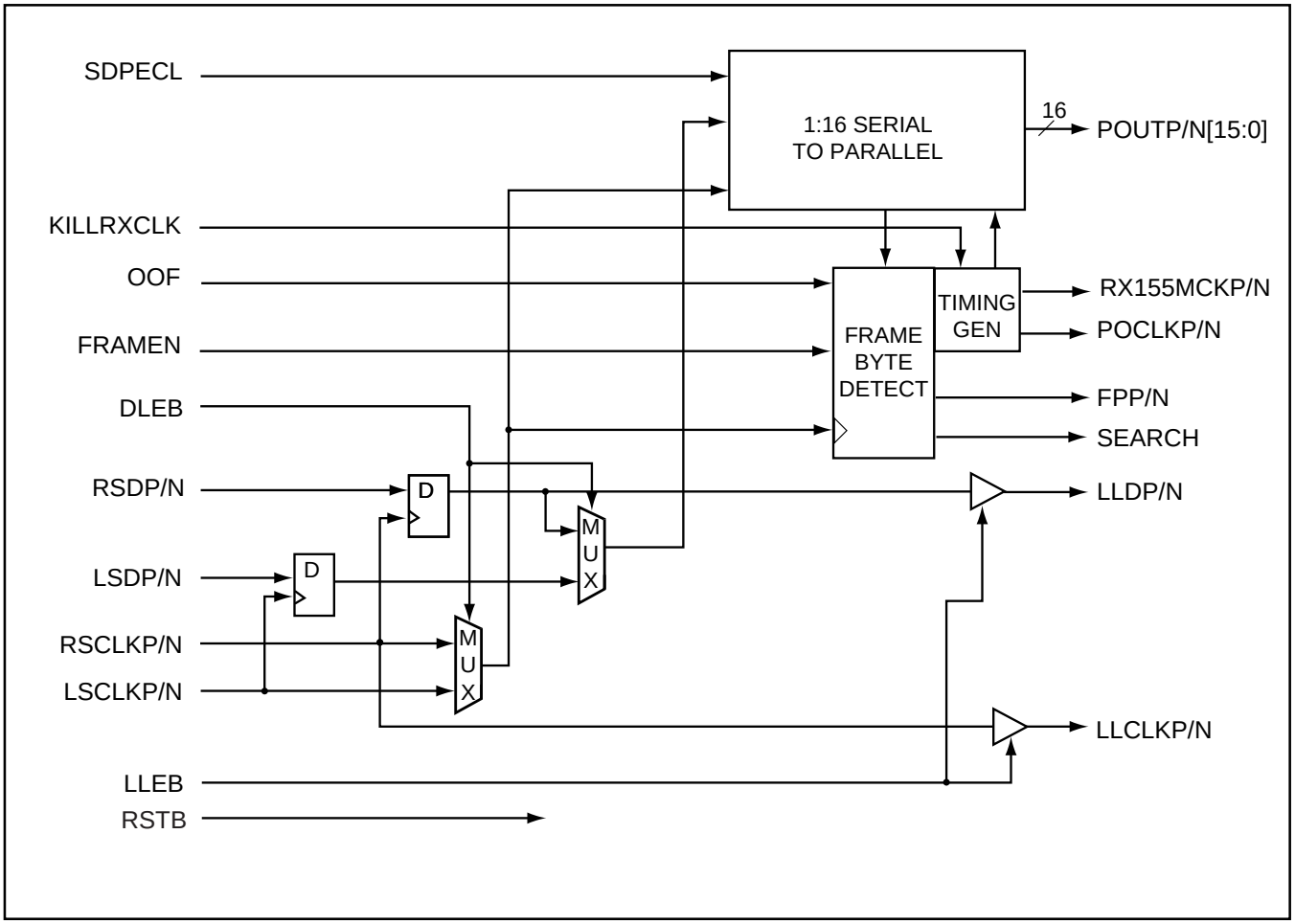
1. Serial input
2. Serial-to-parallel conversion
3. Frame detection
4. 16-bit parallel output

Internal clocking and control functions are transparent to the user. Details of data timing can be seen in Figures 7 through 9. Internal clocking and control functions are transparent to the user.

Suggested Interface Devices

AMCC	S3056	Clock Recovery Device
AMCC	S3063	OC-48 Transmitter

Figure 4. S3064 Functional Block Diagram



RECEIVER OPERATION

The S3064 receiver chip provides the first stage of digital processing of a receive SONET STS-48 bit-serial stream. It converts the bit-serial 2.488 Gbps data stream into a 155.52 Mbyte/sec parallel data format. A loopback mode is provided for diagnostic loopback (transmitter to receiver). A Line Loopback (receiver to transmitter) is also provided.

Frame and Byte Boundary Detection

The Frame and Byte Boundary Detection circuitry searches the incoming data for three consecutive A1 bytes followed immediately by one A2 byte. Framing pattern detection is enabled and disabled by the FRAMEN input. Detection is enabled by a rising edge on OOF when FRAMEN is active. It is disabled when a framing pattern is detected. When framing pattern detection is enabled, the framing pattern is used to locate byte and frame boundaries in the incoming data stream (RSD or looped transmitter data). During this time, the parallel data bus (POUTP/N[15:0]) will not contain valid data. The timing generator block takes the located byte boundary and uses it to block the incoming data stream into bytes for output on the parallel output data bus (POUTP/N[15:0]). The frame boundary is reported on the frame pulse (FP) output when any 32-bit pattern matching the framing pattern is detected on the incoming data stream. When framing pattern detection is disabled, the byte boundary is frozen to the location found when detection was previously enabled. Only framing patterns aligned to the fixed byte boundary are indicated on the FP output.

The probability that random data in an STS-48 stream will generate the 32-bit framing pattern is extremely small. It is highly improbable that a mimic pattern would occur within one frame of data. Therefore, the time to match the first frame pattern and to verify it with down-stream circuitry, at the next occurrence of the pattern, is expected to be less than the required 250 µs, even for extremely high bit error rates.

Serial to Parallel Converter

The serial to parallel converter consists of three 16-bit registers. The first is a serial-in, parallel-out shift register, which performs serial to parallel conversion. The second is an 16-bit internal holding register, which transfers data from the serial to parallel register on byte boundaries as determined by the frame and byte boundary detection block. On the falling edge of the free running POCLK, the data in the holding register is transferred to an output holding register which drives POUTP/N[15:0].

OTHER OPERATING MODES

Diagnostic Loopback

When the Diagnostic Loopback Enable (DLEB) input is active, a loopback from the transmitter to the receiver at the serial data rate can be set up for diagnostic purposes. The differential serial output clock and data from the transmitter (LSCLK and LSD) is routed to the serial-to-parallel block in place of the normal data stream (RSCLK and RSD). When DLEB is asserted, SDPECL shall be ignored.

Line Loopback

The Line Loopback circuitry consists of alternate clock and data output drivers. When LLEB is active, it enables the Line Loopback output data and clock (LLD and LLCLK) and a receive-to-transmit loopback can be established at the serial data rate.

Table 2. Input Pin Assignment and Description

Pin Name	Level	I/O	Pin #	Description
RSDP RSDN	Internally Biased Diff. LVPECL	I	4 5	Receive Serial Data. Serial data stream signals normally connected to an optical receiver module. These inputs are clocked by the RSCLK inputs. Internally biased and terminated.
RSCLKP RSCLKN	Internally Biased Diff. LVPECL	I	8 9	Receive Serial Clock. Recovered clock signal that is synchronous with the RSD inputs. This clock is used by the receive section as the master clock to perform framing and deserialization functions. Internally biased and terminated.
LSDP LSDN	Diff. LVPECL	I	92 91	Loopback Serial Data. Serial data stream signals normally connected to the transmitter for loopback testing. These inputs are clocked by the LSCLK inputs. Internally terminated.
LSCLKP LSCLKN	Diff. LVPECL	I	100 99	Loopback Serial Clock. Clock input from the transmitter that is synchronous with the LSD inputs. This clock is used during local loopback testing to perform the framing and deserialization functions. Internally terminated.
OOF	LVTTL	I	17	Out of Frame. Indicator used to enable framing pattern detection logic in the S3064. The framing pattern detection logic is enabled by a rising edge on OOF, and remains enabled until frame boundary is detected. OOF is an asynchronous signal with a minimum pulse width of one POCLK period. (See Figures 10 and 11.)
SDPECL	Single-Ended LVPECL	I	20	LVPECL Signal Detect. Active High. A single-ended LVPECL input to be driven by the external optical receiver module to indicate a loss of received optical power. When SDPECL is inactive, the data on the Serial Data In (RSDP/N) pins will be internally forced to a constant zero. When SDPECL is active, data on the RSDP/N pins will be processed normally. SDPECL will not affect the serial data path when DLEB is active.
DLEB	LVTTL	I	22	Diagnostic Loopback Enable. Selects diagnostic loopback. Active Low. When DLEB is inactive, the S3064 device uses the primary data (RSD) and clock (RSCLK) inputs. When active, the S3064 device uses the diagnostic loopback clock and data from the transmitter.
RSTB	LVTTL	I	25	Master Reset. Reset input for the device. Active Low. During reset, POCLK does not toggle.
LLEB	LVTTL	I	21	Line Loopback Enable. Selects Line Loopback. Active Low. When LLEB is active, the S3064 will enable the data from the LLD/LLCLK outputs.
KILLRXCLK	LVTTL	I	19	Kill Receive Clock Input. For normal operation set KILLRXCLK "High." When this input is low, it will force RX155 MCK and POCLK outputs to a logic "0" state.
FRAMEN	LVTTL	I	18	Frame Enable Input. For normal operation set FRAMEN High. This enables the frame detector circuit to detect A1 A2 alignment and lock to word boundary. When this input is Low, it will disable the frame detector circuit and it will lock on the last byte alignment state.

Table 3. Output Pin Assignment and Description

Pin Name	Level	I/O	Pin #	Description
POUTP0 POUTN0 POUTP1 POUTN1 POUTP2 POUTN2 POUTP3 POUTN3 POUTP4 POUTN4 POUTP5 POUTN5 POUTP6 POUTN6 POUTP7 POUTN7 POUTP8 POUTN8 POUTP9 POUTN9 POUTP10 POUTN10 POUTP11 POUTN11 POUTP12 POUTN12 POUTP13 POUTN13 POUTP14 POUTN14 POUTP15 POUTN15	Diff. LVPECL	O	33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 54 55 56 57 58 59 60 61 62 63 64 65 66 67	Parallel Output. Parallel data bus, a 155.52 Mbyte/sec 16-bit word, aligned to the parallel output clock (POCLK). POUT[15] is the most significant bit (corresponding to bit 1 of each PCM word, the first bit received). POUT[0] is the least significant bit (corresponding to bit 16 of each PCM word, the last bit received). POUT[15:0] is updated on the falling edge of POCLK.
LLDP LLDN	Low Swing Diff. CML	O	77 76	Line Loopback Data. A retimed version of the incoming data stream [RSD]. Enabled by LLEB.
LLCLKP LLCLKN	Diff. CML	O	86 85	Line Loopback Clock. A buffered version of the RSCLK or LSCLK input. Enabled by LLEB.

Table 3. Output Pin Assignment and Description (Continued)

Pin Name	Level	I/O	Pin #	Description
FPP FPN	Diff. LVPECL	O	31 32	Frame Pulse. Indicates frame boundaries in the incoming data stream. If framing pattern detection is enabled, as controlled by the OOF input, FP pulses high for one POCLK cycle when a 32-bit sequence matching the framing pattern is detected on the serial data inputs. When framing pattern detection is disabled, FP pulses high when the incoming data stream, after byte alignment, matches the framing pattern. FP is updated on the falling edge of POCLK.
POCLKP POCLKN	Diff. LVPECL	O	68 69	Parallel Output Clock. A 155.52 MHz nominally 50% duty cycle, byte rate output clock, that is aligned to POUTP/N[15:0] byte serial output data. POUTP/N[15:0] and FP are updated on the falling edge of POCLK.
SEARCH	LVTTL	O	26	A1 A2 Frame Search Output. A High on this output pin indicates the frame detection circuit is activated and it is searching for a new A1 A2 byte alignment. This output will be High during the entire period of A1 A2 frame search. Once a new alignment is found, this signal will remain High for a minimum of one 155.52 MHz clock period beyond the third A2 byte before it will be set to Low.
RX155MCKP RX155MCKN	Diff. LVPECL	O	29 30	Receive Free Running 155.52 MHz Clock Output. This clock is generated by dividing the RSCLK signal by sixteen.

Table 4. Common Pin Assignment and Description

Pin Name	Level	I/O	Pin #	Description
CORE_GND	GND		11, 13, 15, 72, 87, 88	Core Ground
CORE_VCC	+3.3V		10, 12, 14, 73, 89, 90	Core VCC
LVP_VCC	+3.3V		1, 6, 27, 53, 71, 79, 83, 84, 94, 97, 98	LVPECL VCC
LVP_GND	GND		2, 3, 7, 28, 51, 52, 70, 78, 81, 82, 93, 95, 96	LVPECL Ground
TTL_VCC	+3.3V		16	TTL VCC
TTL_GND	GND		24	TTL Ground
THD			23	Thermal Diode
NC			74, 75, 80	Not Connected

Figure 5. S3064 Pinout

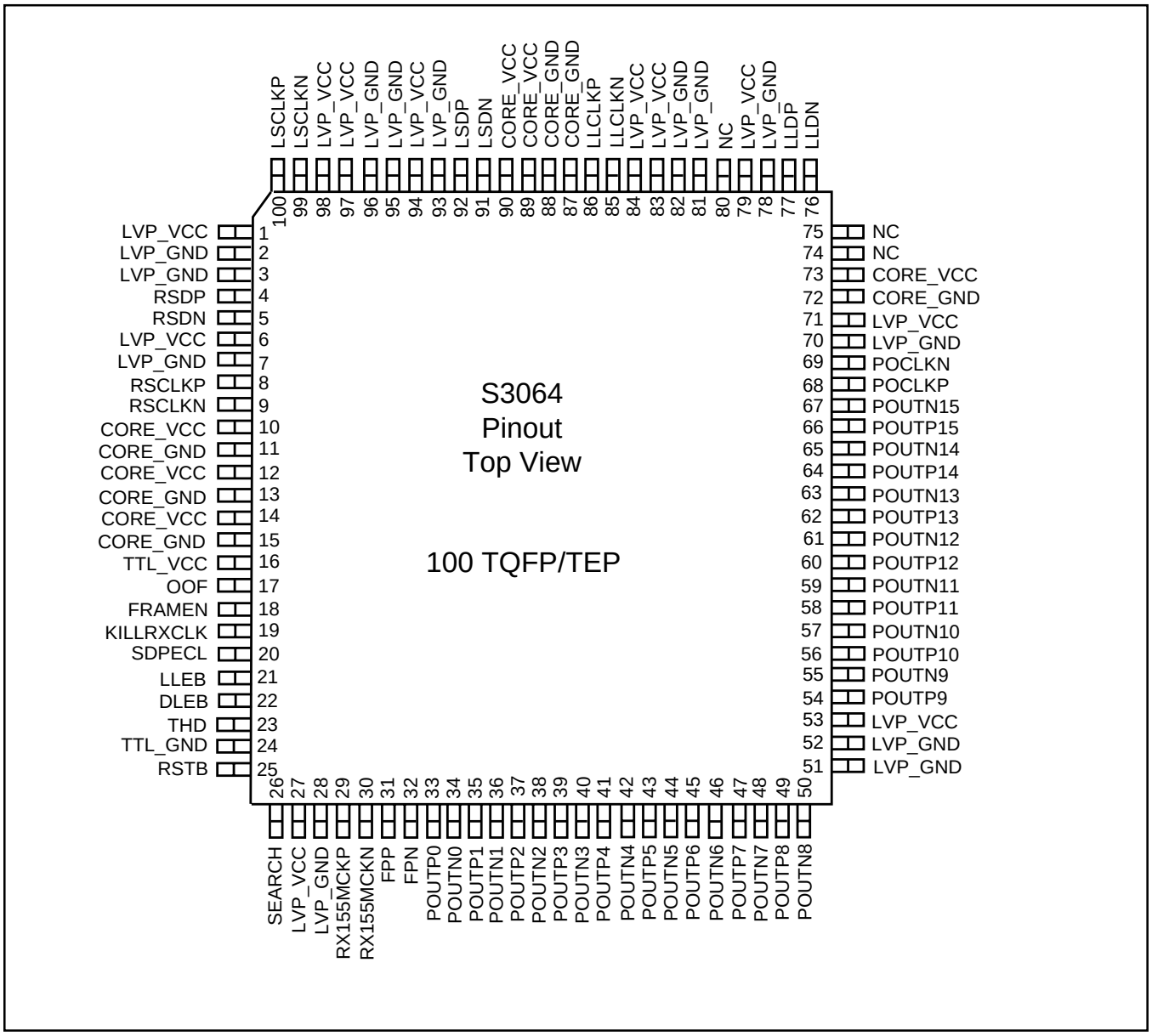
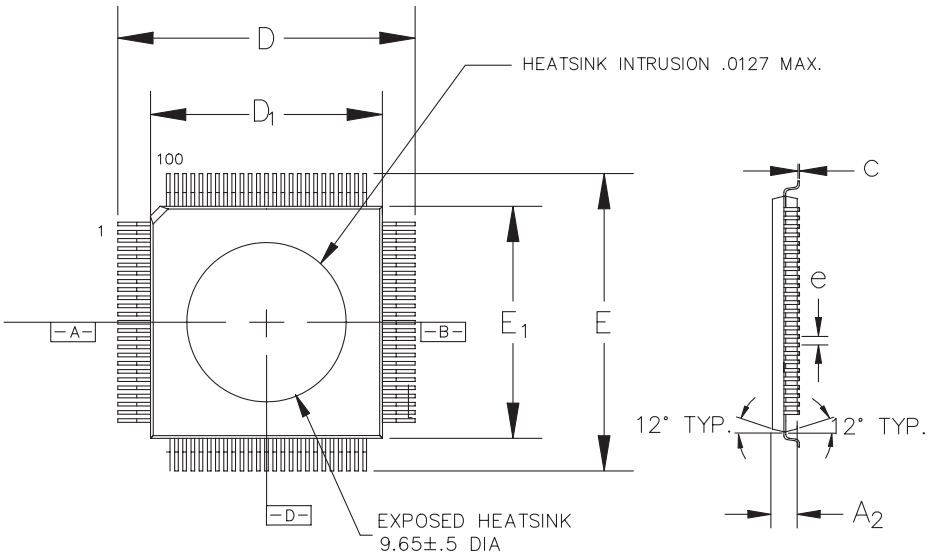
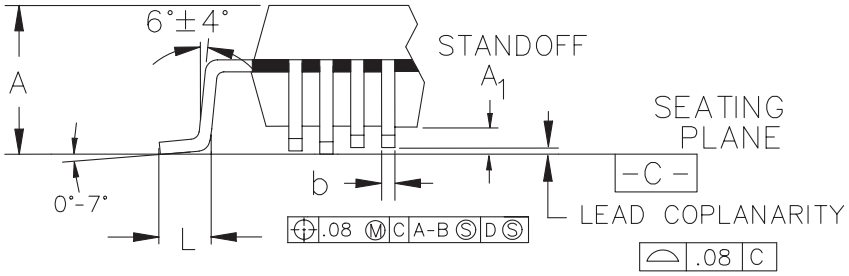


Figure 6. 100 TQFP/TEP Package





DIMENSIONS (are in millimeters)

UNIT	A	A_1	A_2	D	D_1	E	E_1	L	b	e	c
MIN		0.05	1.35	15.80	13.95	15.80	13.95	0.50	0.17	0.50 BSC.	
NOM			1.40	16.00	14.00	16.00	14.00	0.60	0.22		
MAX	1.60	0.15	1.45	16.20	14.05	16.20	14.05	0.75	0.27		0.17

Thermal Management

Device	Max Power	Θjc
S3064	1.32 W	2.5˚C/W

1. Add 45 mA for loopback active.
2. Open outputs.

Note: The S3064 package is equipped with an embedded conductive heatsink on the top (board side).

Table 5. Absolute Maximum Ratings

Parameter	Min	Typ	Max	Units
Storage Temperature	-65		150	˚C
Voltage on Vcc with Respect to GND	-0.5		+5.0	V
Voltage on any LVPECL Input Pin	0		V_{CC}	V
Voltage on any LVTTL Input Pin	-0.5		+5.5	V
High Speed LVPECL Output Source Current			50	mA

ESD Ratings

The S3064 is rated to the following voltages based on the human body model:
1. All pins are rated at or above 2000 V except THD, LSCLKP/N, LSDP/N, LLDP/N.

Table 6. Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Case Temperature Under Bias	0		100	˚C
Voltage on V_{CC} with Respect to GND	3.13	3.3	3.47	V
Voltage on any LVPECL Input Pin	V_{CC} -2		V_{CC}	V
Voltage on any LVTTL Pin	0		3.47	V

Table 7. Power Consumption

Parameter	Min	Typ	Max	Units
I_{CC} [1,2]		300	380	mA

1. Add 45mA for loopback active.
2. Open outputs.

Table 8. Low Swing Differential CML Output DC Characteristics

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OL}	Low Swing CML Output LOW Voltage	V_{CC} -0.55		V_{CC} -0.25	V	100Ω line-to-line.
V_{OH}	Low Swing CML Output HIGH Voltage	V_{CC} -0.25		V_{CC} -0.05	V	100Ω line-to-line.
$\Delta V_{OUTDIFF}$ (Data)	Low Swing CML Serial Output Differential Voltage Swing	360		800	mV	100Ω line-to-line.
$\Delta V_{OUTSINGLE}$ (Data)	Low Swing CML Serial Output Single-ended Voltage Swing	180		400	mV	100Ω line-to-line.

Table 9. Differential CML Output DC Characteristics

Parameter	Description	Min	Typ	Max	Units	Condition
V_{OL}	CML Output LOW Voltage	V_{CC} -1.05		V_{CC} -0.55	V	100Ω line-to-line.
V_{OH}	CML Output HIGH Voltage	V_{CC} -0.45		V_{CC} -0.10	V	100Ω line-to-line.
$\Delta V_{OUTDIFF}$ Clock	CML Serial Output Differential Voltage Swing	700		1300	mV	100Ω line-to-line. See Figure 13.
$\Delta V_{OUTSINGLE}$ Clock	CML Serial Output Single-ended Voltage Swing	350		650	mV	100Ω line-to-line. See Figure 13.

Table 10. Internally Biased Differential LVPECL Input DC Characteristics

Parameters	Description	Min	Typ	Max	Units	Conditions
ΔV_{INDIFF}	Differential Input Voltage Swing	300		1200	mV	See Figure 13.
$\Delta V_{INSINGLE}$	Differential Input Single-Ended Swing	150		600	mV	See Figure 13.
R_{DIFF}	Differential Input Resistance	80	100	120	Ω	

Table 11. Differential LVPECL Input DC Characteristics

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{IL}	LVPECL Input LOW Voltage	V_{CC} -2.000		V_{CC} -0.25	V	
V_{IH}	LVPECL Input HIGH Voltage	V_{CC} -1.20		V_{CC} -0.05	V	
ΔV_{INDIFF}	Differential Input Voltage Swing	300		1200	mV	See Figure 13.
$\Delta V_{INSINGLE}$	Differential Input Single-Ended Swing	150		600	mV	See Figure 13.
R_{DIFF}	Differential Input Resistance	80	100	120	Ω	

Table 12. Single Ended LVPECL Input DC Characteristics[1]

Parameters	Description	Min	Max	Units	Conditions
V_{IL}	PECL Input Low Voltage	V_{CC} -2.30	V_{CC} -1.44	V	Guaranteed at +85˚ C.
		V_{CC} -2.30	V_{CC} -1.50	V	Guaranteed at -40˚ C.
V_{IH}	PECL Input High Voltage	V_{CC} -1.02	V_{CC} -0.57	V	Guaranteed at +85˚ C.
		V_{CC} -1.22	V_{CC} -0.57	V	Guaranteed at -40˚ C.
I_{IH}	Input High Current		20	µA	
I_{IL}	Input Low Current	-0.5		µA	

1. The AMCC LVPECL inputs are non-temperature compensated I/O which vary at 1.3 mV/C˚.

Table 13. Low Speed Differential LVPECL Output DC Characteristics

Parameters	Description	Min	Max	Units	Comments
$\Delta V_{OUTSINGLE}$	Single Ended Output Voltage Swing	320	950	mV	220Ω to GND and100Ω line-to-line. See Figure 13.
$\Delta V_{OUTDIFF}$	Diff. Output Voltage Swing	640	1900	mV	220Ω to GND and100Ω line-to-line. See Figure 13.
V_{OH}	Output High Voltage	V_{CC} -1.15	V_{CC} -0.60	V	220Ω to GND and100Ω line-to-line.
V_{OL}	Output Low Voltage	V_{CC} -1.95	V_{CC} -1.45	V	220Ω to GND and100Ω line-to-line.
R_{LOAD}		220		Ω	

Table 14. LVTTL Input/Output DC Characteristics

Symbol	Description	Min	Max	Unit	Conditions
V_{IH}	Input High Voltage	2.0	TTL V_{CC}	V	TTL V_{CC} = Max
V_{IL}	Input Low Voltage	0.0	0.8	V	TTL V_{CC} = Max
I_{IH}	Input High Current		50	µA	V_{IN} = 2.4 V
I_{IL}	Input Low Current	-500		µA	V_{IN} = 0.5 V
V_{OH}	Output High Voltage	2.2		V	V_{IH} = Min V_{IL} = Max I_{OH} = -100 µA
V_{OL}	Output Low Voltage		0.5	V	V_{IH} = Min V_{IL} = Max I_{oL} = 4 mA

Table 16. AC Receiver Timing Characteristics

Symbol	Description	Min	Max	Units
(note 1,3)	POCLK Duty Cycle	45	55	%
tP_{POUT}[1]	POCLK Low to POUT [15:0] Valid Prop. Delay	-1	+1	ns
tS_{POUT}[1]	POUT[15:0] and FP Set-up Time w.r.t. POCLK	2		ns
tH_{POUT}[1]	POUT[15:0] and FP Hold Time w.r.t. POCLK	2		ns
tS_{RSD}[2]	RSDP/N Set-up Time w.r.t. RSCLKP/N	75		ps
tH_{RSD}[2]	RSDP/N Hold Time w.r.t. RSCLKP/N	75		ps
tS_{LLD}	LLDP/N Set-Up Time w.r.t. LLCLKP/N	150		ps
tH_{LLD}	LLDP/N Hold Time w.r.t. LLCLKP/N	70		ps
(note 2)	RSCLK/LSCLK Clock Period	400		ps
(note 2,3)	RSCLK Clock Duty Cycle	45	55	%
(note 1)	POUT [15:0] Rise and Fall Time		1.0	ns
(note 2,3)	LSCLK Duty Cycle	40	60	%
	Set-up time for LSDP/N w.r.t. LSCLK		75	ps
	Hold Time for LSCLKP/N w.r.t. LSCLK		75	ps

1. 220Ω to GND and 100Ω line-to-line.
2. 100Ω line-to line.
3. Zero crossing to zero crossing.

Figure 7. Output Timing Diagram

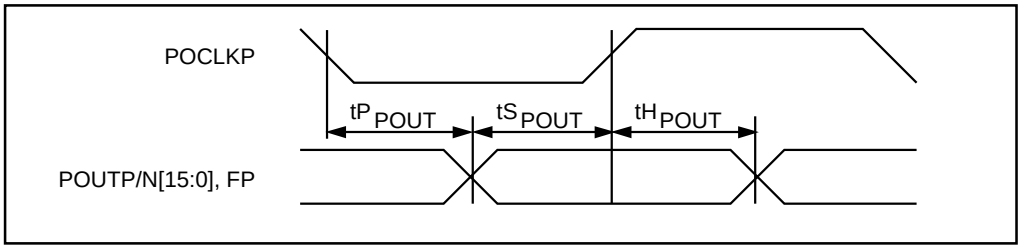
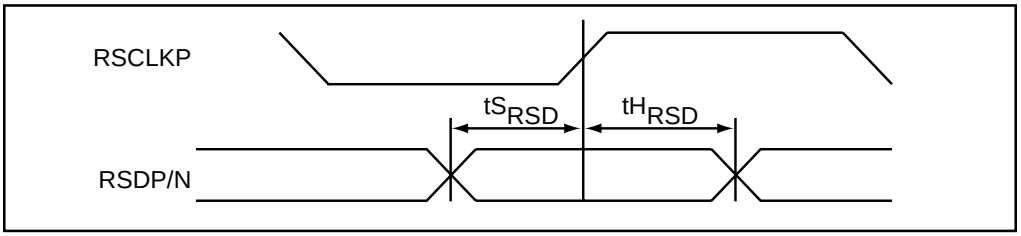


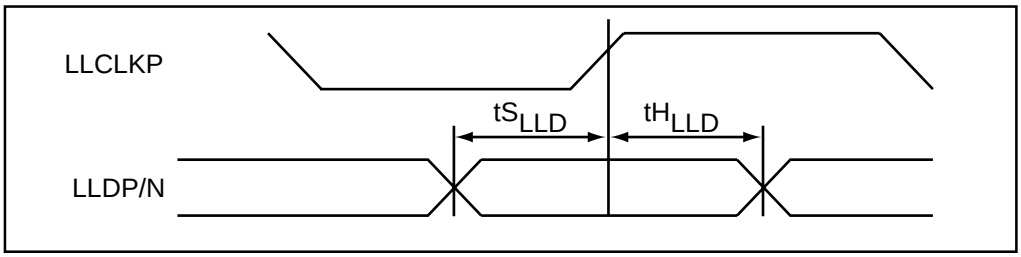
Figure 8. Receiver Input Timing Diagram



Notes on High-Speed LVPECL Input Timing:

1. Timing is measured from the cross-over point of the reference signal to the cross-over point of the input.

Figure 9. LLD Output Timing



RECEIVER FRAMING

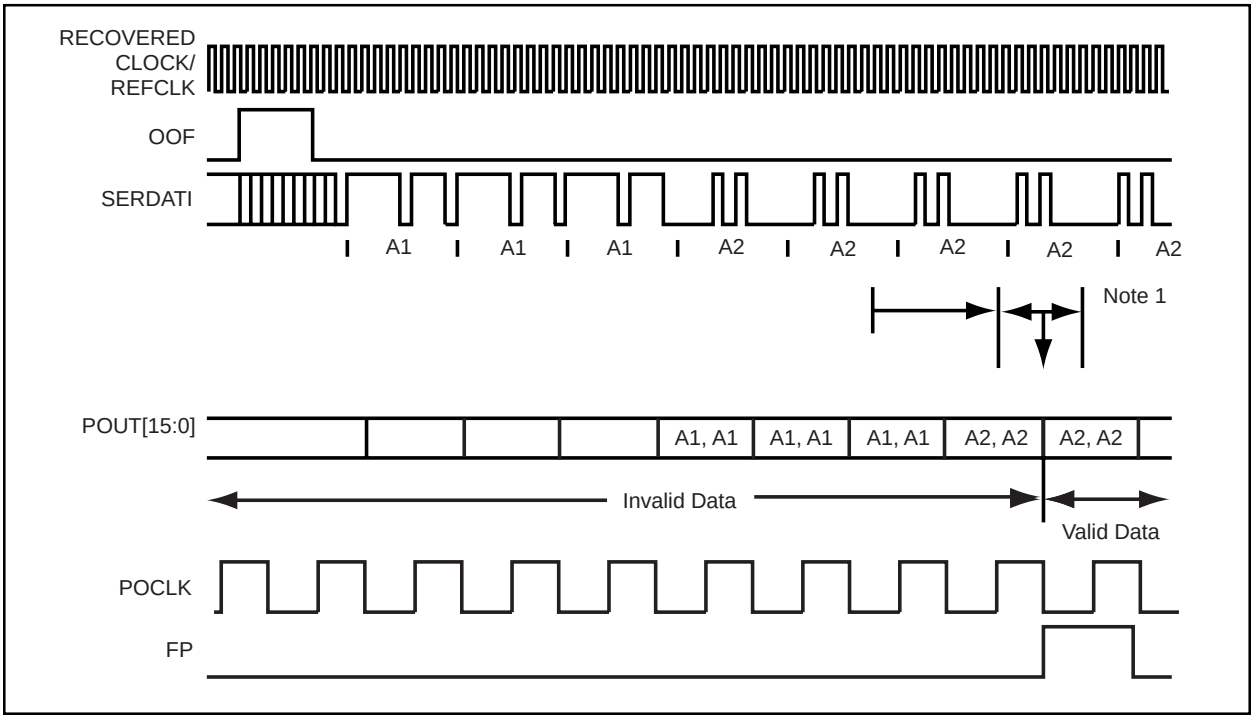
Figure 10 shows a typical reframe sequence in which a byte realignment is made. The frame and byte boundary detection is enabled by the rising edge of OOF. Both boundaries are recognized upon receipt of the first A2 byte. The third A2 byte is the first data byte to be reported with the correct byte alignment on the outgoing data bus (POUTP/N[15:0]). Concurrently, the frame pulse is set high for one POCLK cycle.

The frame and byte boundary detection block is activated by the rising edge of OOF, and stays active until the first FP pulse.

Figure 11 shows the frame and byte boundary detection activation by a rising edge of OOF, and deactivated by the first FP pulse.

Figure 12 shows the frame and byte boundary detection activation by a rising edge of OOF, and deactivated by the FRAMEN input.

Figure 10. Frame and Byte Detection



1. Range of input to output delay can be 1.5 to 2.5 POCLK cycles.

Figure 11. OOF Timing (FRAMEN = 1)

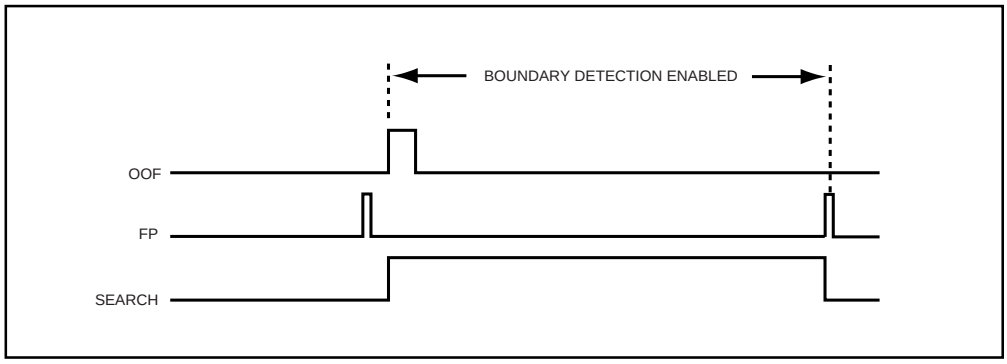


Figure 12. FRAMEN Timing

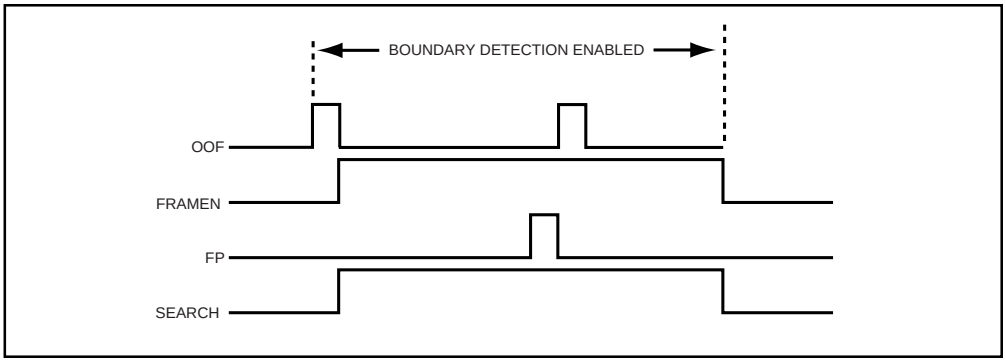
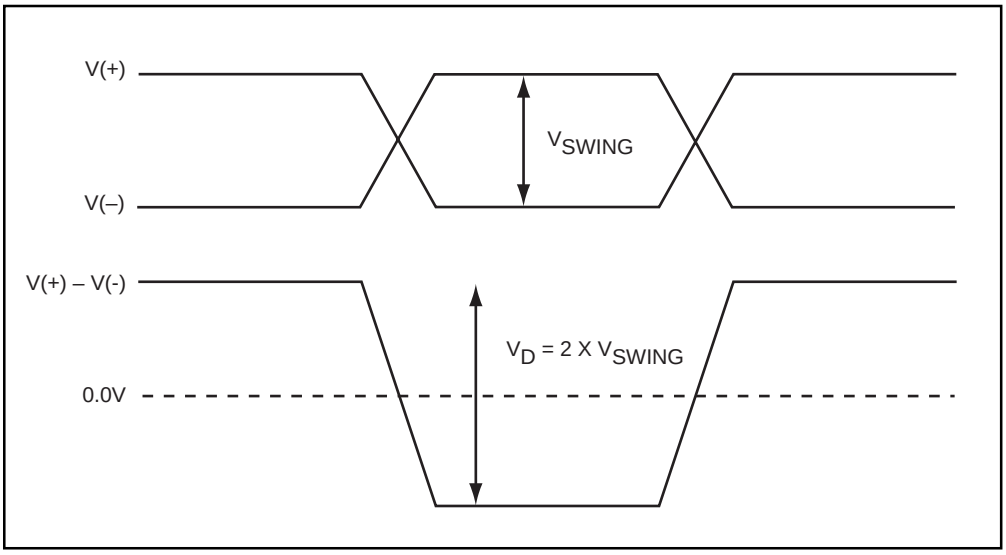


Figure 13. Differential Voltage Measurement



Note: V(+) – V(-) is the algebraic difference of the input signals.

Figure 14. +5V Differential PECL Driver to S3064 Internally Biased Differential LVPECL Input AC Coupled Termination

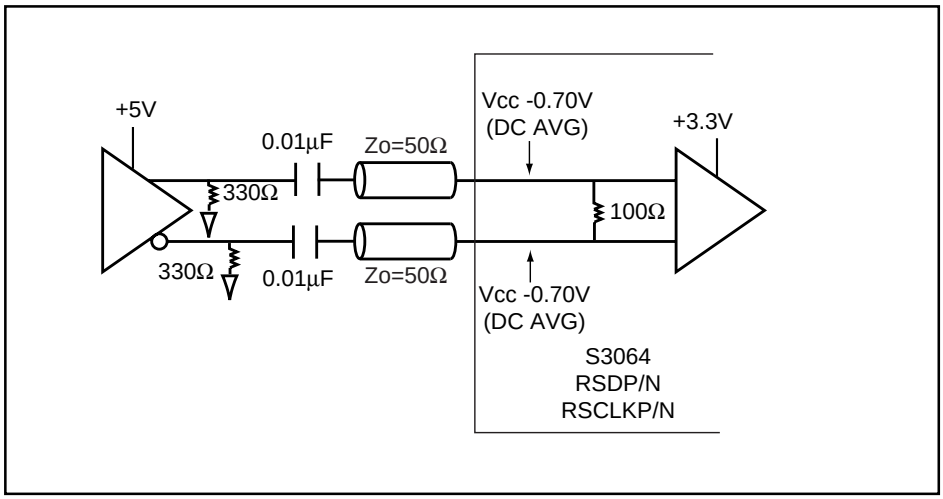


Figure 15. S3056 to S3064 Internally Biased Differential LVPECL Input DC Terminations

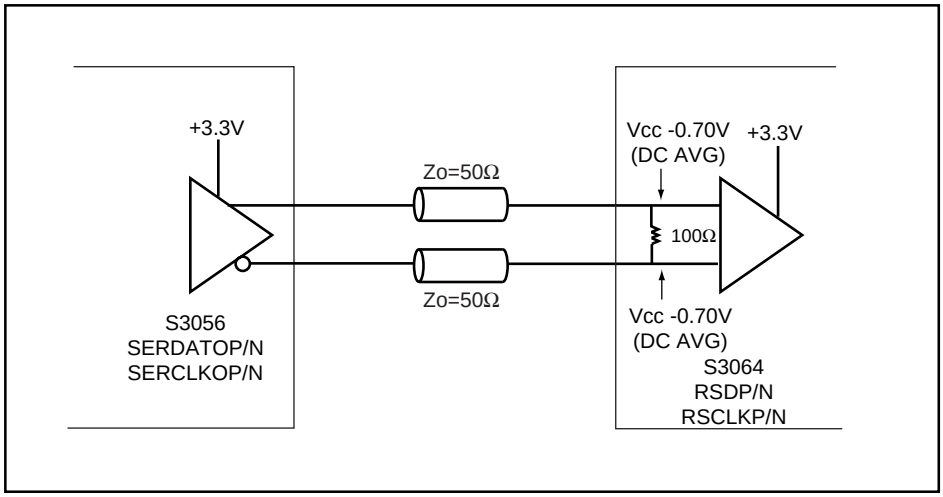


Figure 16. S3064 Differential CML Output to S3063 Terminations

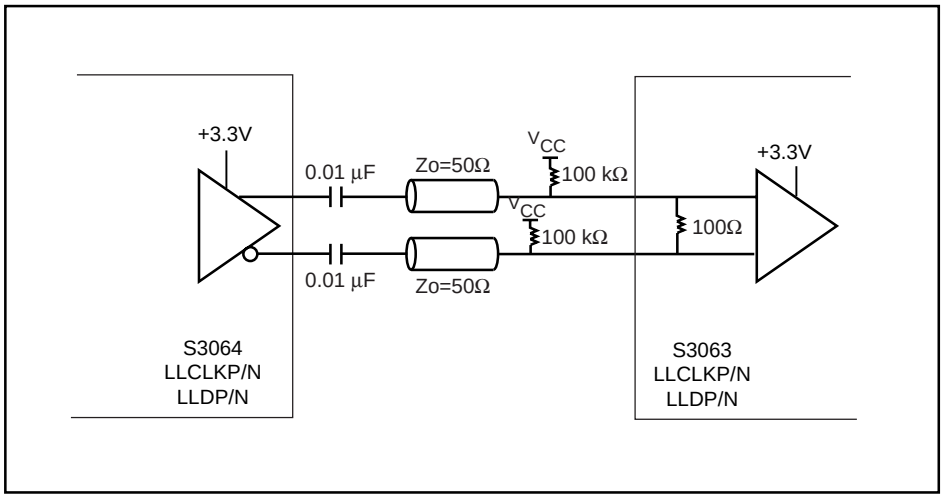


Figure 17. S3064 Differential PECL Output

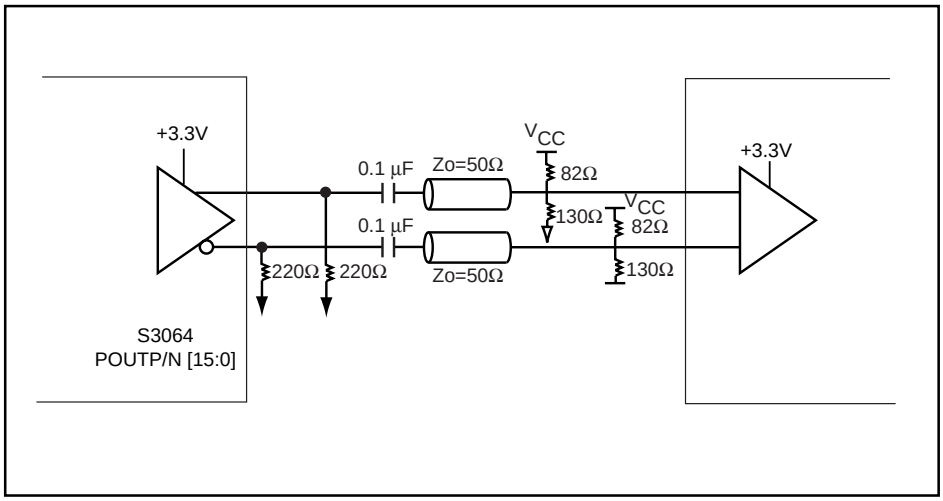


Figure 18. Differential PECL Output Termination

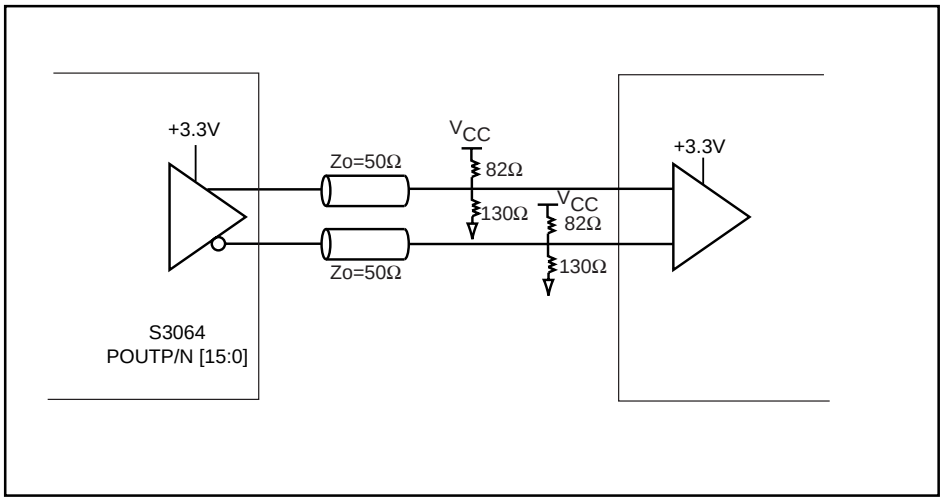


Figure 19. Differential PECL Output Termination to S3064 Internally Biased Differential LVPECL Input DC Terminations

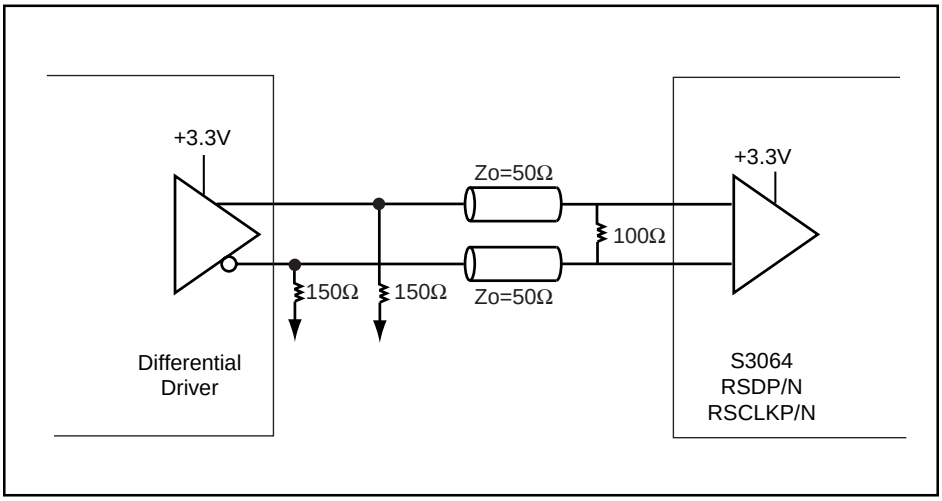


Figure 20. S3063 to S3064 for Diagnostic Loopback

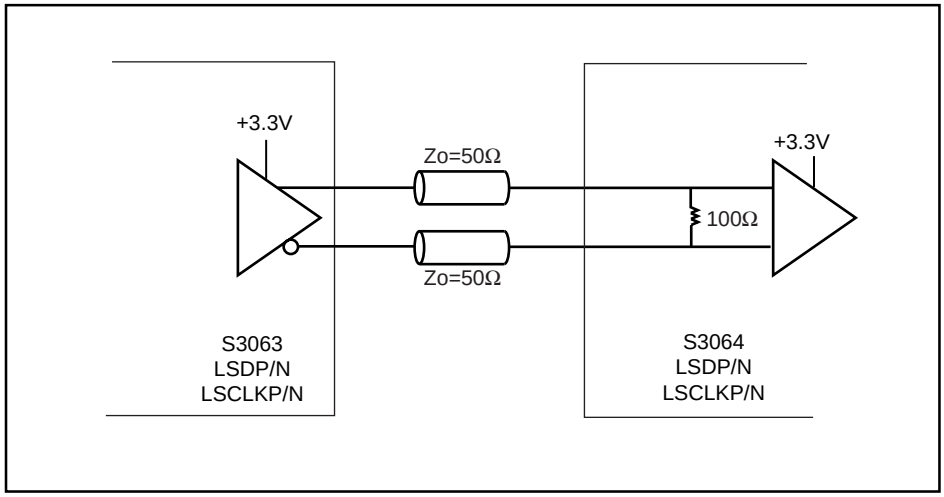
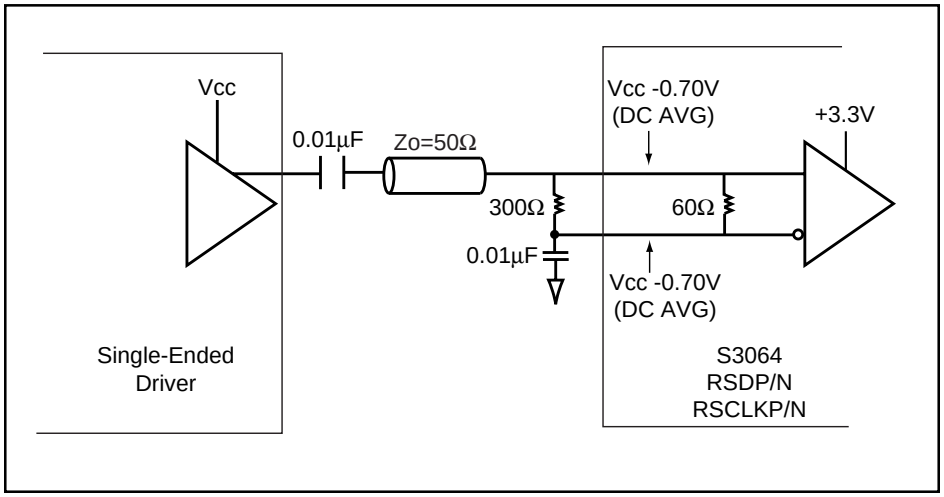
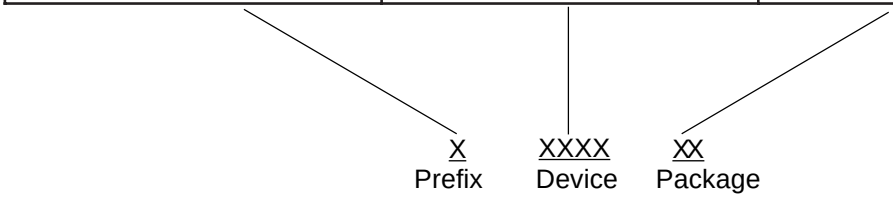


Figure 21. Single-Ended LVPECL Driver to S3064 Input AC Coupled Termination



Ordering Information

PREFIX	DEVICE	PACKAGE
S – Integrated Circuit	3064	TT – 100 TQFP/TEP



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