S3083, S3044, S3056 and S4802 MISSOURI with Sumitomo Fiber Optics

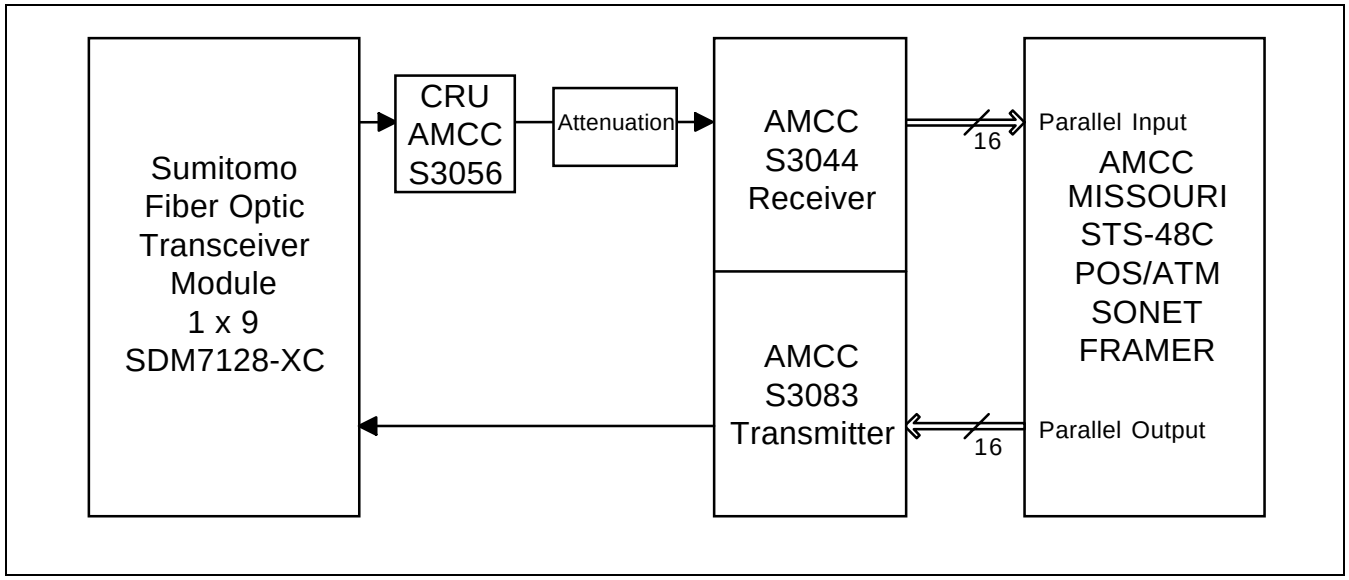
OC-48 APPLICATION NOTE

AMCC S3083 Transmitter, S3044 Receiver, S3056 CDR, Sumitomo SDM7128-XC Fiber Optic Transceiver and AMCC MISSOURI S4802 POS/ATM SONET Framer

Introduction

The AMCC S3083 transmitter and S3044 receiver chips are fully integrated serialization/deserialization SONET STS-48/OC-48 (2.488 Gbps) interface devices. These devices are suitable for SONET based ATM applications, and can be used in conjunction with AMCC's S3056 Clock Recovery Unit (CRU). The AMCC S3083 and S3044 chips provide the first stage of the digital processing of a receive and a transmit SONET STS-48 bit-serial stream. In the receive path the S3044 converts a OC-48 bit-serial data stream into a 16-bit 155.52 Mbps parallel data format and performs frame and byte detection. In the transmit path the S3083 converts 16-bit parallel data into bit-serial data at 2.488 Gbps. The S3083 chip can be used with a 155.52 MHz reference clock in support of existing system clock schemes. Figure 1 shows a typical application block diagram with an AMCC MISSOURI. Figure 2 shows more design details. Combining these devices provides a Physical Media Dependent (PMD) layer for SONET/SDH data transfer.

Figure 1. Typical Network Application Block Diagram

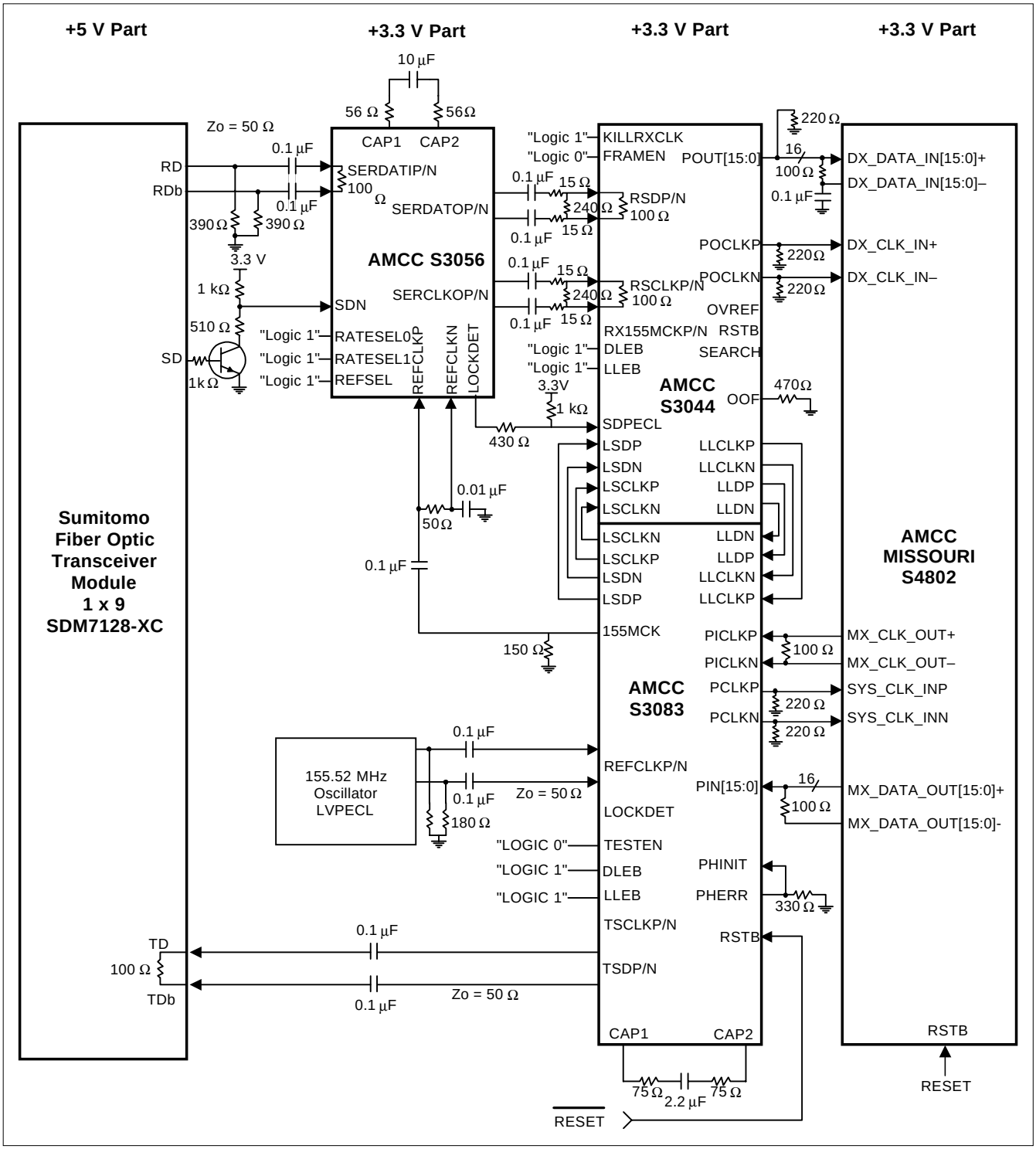


Signal Connect Description

Figure 1 shows the block diagram of this solution.

1. The Sumitomo fiber optic transceiver interfaces to the AMCC S3056 CRU chip via a bit-serial data stream.
2. After the clock is recovered from the bit-serial data stream the CRU chip transmits the recovered clock and re-timed data to the AMCC S3044 receiver.
3. The S3044 receiver transmits the bit-serial data converted into 16-bit parallel data to the MISSOURI.
4. The MISSOURI transmits 16-bit parallel data to the AMCC S3083.
5. The S3083 transmits the bit-serial data to the Sumitomo fiber optic transceiver.

Figure 2. S3083 Transmitter, S3044 Receiver, S3056 CDR, Sumitomo SDM7128-XC Fiber Optic Transceiver and AMCC MISSOURI S4802 POS/ATM SONET Framer



Theory of Operation

1. The S3056 extracts the clock and re-times the data from the received differential CML Serial Data Input (SERDATIP/N) coming from the fiber optic receiver when the Signal Detect (SDN) is an LVPECL Low level. When Signal Detect (SDN) is at an LVPECL High level, the Phase Lock Loop (PLL) will be forced to lock to the differential LVPECL Reference Clock (REFCLKP/N). When the transmit PLL is locked to the reference clock input the Lock Detect (LOCKDET) LVTTL output goes High.
2. The S3044 receives the OC-48 (2.488 Gbit/s) scrambled NRZ data signals on the Receive Serial Data stream (RSDP/N) differential LVPECL inputs. These inputs are clocked into the S3044 by the Receive Serial Clock (RSCLKP/N) differential LVPECL inputs. This clock is used by the receive section as the master clock to perform framing and deserialization functions.
3. When FRAMEN is disabled [FRAMEN = 0] and OOF is connected to ground, the Frame Pulse (FP) output is always inactive. The MISSOURI device should be in default mode [RX_FRMR_INH = 0]. In this mode, the parallel input data is not assumed to be byte aligned. The MISSOURI device will align to the incoming data.
4. The serial-bit data stream is then converted into a 16-bit parallel data format for output onto the Parallel Output data bus (POUT[15:0]). The 16-bit parallel data is clocked out of the S3044 and into the AMCC MISSOURI S4802 with the Parallel Output Clock (POCLK).
5. The 16-bit parallel data is output from the AMCC MISSOURI S4802 into the S3083 parallel data input bus (PIN[15:0]) and is sampled by the Parallel Input Clock (PICLK) of the S3083. This clock is generated by the S3083 Parallel Clock (PCLK) which is fed into the AMCC MISSOURI S4802 as the transmit clock (MX_CLK_OUT) and then back into the PICLK input of the S3083.
6. The 16-bit parallel data is then converted to bit-serial data and output through the Transmit Serial Data (TSDP/N) connections to the Sumitomo fiber optic transmitter (SDM7128-XC).
7. If the incoming serial-bit data stream is lost (when SDN is High) the lock detect circuit internal to the S3056 substitutes the external reference clock for the missing data stream clocking signal. This substitution of reference timing source is helpful to supply a continuous timing signal for the upstream devices and system operation even though valid received data does not exist. This switch over is a smooth transition with no noticeable phase shift.

Terminations

The following is a list of terminations that need to be added for this particular design.

1. The 100 Ω line to line termination resistor should be as close to the termination points as possible.
2. The 330 Ω and 390 Ω pull down resistors should be as close to the sources as possible.
3. The high frequency traces should be designed as 50 Ω transmission lines with the termination as depicted in Figure 2.
4. All the termination resistors should be placed at the end of the transmission line, and the power supply decoupling should be placed as close as possible to the devices.
5. The PECL and LVPECL (differential pairs) traces should have equal length, (allows both signals to arrive at the destination at the same time) and be run in parallel and in close proximity of one another. This allows the same noise to couple onto both of the lines and become common mode noise which is ignored by differential inputs.
6. Separate resets should be used for the S3083 and S4802 MISSOURI. During RESET, the PCLK of the S3083 is disabled. The MISSOURI requires TX_SONETCLK from PCLK to run for proper reset of the device. MISSOURI requires approximately 10-15 clock cycles to reset.

Conclusion

The Sumitomo fiber optic transceiver, AMCC's S3083/S3044/S3056 and the AMCC MISSOURI S4802 solution combine to make a complete OC-48 Physical Media Dependent (PMD) layer for SONET/SDH data transfer.

Disclaimer

The circuit presented in this application note is based on data sheet information as well as standard implementation of termination schemes. It has not been built and tested in the lab environment.

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