NTD3055-150

Power MOSFET
9.0 Amps, 60 Volts

N-Channel DPAK

Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls and bridge circuits.

Typical Applications

- Power Supplies
- Converters
- Power Motor Controls
- Bridge Circuits

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	60	Vdc
Drain-to-Gate Voltage (R_{GS} = 10 MΩ)	V_{DGR}	60	Vdc
Gate-to-Source Voltage - Continuous - Non-repetitive ($t_p \leq 10$ ms)	 V_{GS} V_{GS}	 ±20 ±30	Vdc
Drain Current - Continuous @ T_A = 25°C - Continuous @ T_A = 100°C - Single Pulse ($t_p \leq 10$ μs)	 I_D I_D I_{DM}	 9.0 3.0 27	Adc Apk
Total Power Dissipation @ T_A = 25°C Derate above 25°C Total Power Dissipation @ T_A = 25°C (Note 1) Total Power Dissipation @ T_A = 25°C (Note 2)	P_D	28.8 0.19 2.1 1.5	W W/°C W W
Operating and Storage Temperature Range	T_J, T_{stg}	- 55 to 175	°C
Single Pulse Drain-to-Source Avalanche Energy - Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 10 Vdc, L = 1.0 mH, I_L(pk) = 7.75 A, V_{DS} = 60 Vdc)	E_{AS}	30	mJ
Thermal Resistance - Junction-to-Case - Junction-to-Ambient (Note 1) - Junction-to-Ambient (Note 2)	 $R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	 5.2 71.4 100	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

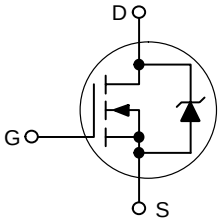
1. When surface mounted to an FR4 board using 0.5 sq. in pad size.
2. When surface mounted to an FR4 board using minimum recommended pad size.

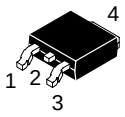
ON Semiconductor™

http://onsemi.com

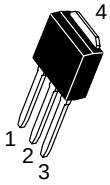
9.0 AMPERES
60 VOLTS
$R_{DS(on)}$ = 122 mΩ (Typ)

N-Channel



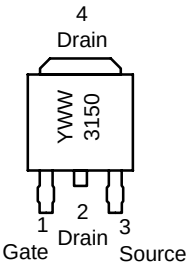


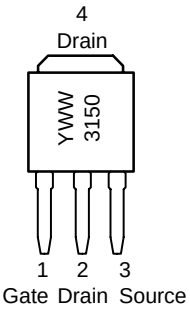
DPAK
CASE 369C
(Surface Mount)
Style 2



DPAK
CASE 369D
(Straight Lead)
Style 2

MARKING DIAGRAMS





3150	Device Code
Y	= Year
WW	= Work Week

ORDERING INFORMATION

Device	Package	Shipping
NTD3055-150	DPAK	75 Units/Rail
NTD3055-150-1	DPAK Straight Lead	75 Units/Rail
NTD3055-150T4	DPAK	2500/Tape & Reel

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage (Note 3) (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	60 -	- 70.2	- -	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc, T_J = 150°C)		I_{DSS}	- -	- -	1.0 10	μAdc
Gate-Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	-	-	±100	nAdc
ON CHARACTERISTICS (Note 3)						
Gate Threshold Voltage (Note 3) (V_{DS} = V_{GS}, I_D = 250 μAdc) Threshold Temperature Coefficient (Negative)		$V_{GS(th)}$	2.0 -	3.0 6.4	4.0 -	Vdc mV/°C
Static Drain-to-Source On-Resistance (Note 3) (V_{GS} = 10 Vdc, I_D = 4.5 Adc)		$R_{DS(on)}$	-	122	150	mΩ
Static Drain-to-Source On-Voltage (Note 3) (V_{GS} = 10 Vdc, I_D = 9.0 Adc) (V_{GS} = 10 Vdc, I_D = 4.5 Adc, T_J = 150°C)		$V_{DS(on)}$	- -	1.4 1.1	1.9 -	Vdc
Forward Transconductance (Note 3) (V_{DS} = 7.0 Vdc, I_D = 6.0 Adc)		g_{FS}	-	5.4	-	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	-	200	280	pF
Output Capacitance		C_{oss}	-	70	100	
Transfer Capacitance		C_{rss}	-	26	40	
SWITCHING CHARACTERISTICS (Note 4)						
Turn-On Delay Time	(V_{DD} = 48 Vdc, I_D = 9.0 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω) (Note 3)	$t_{d(on)}$	-	11.2	25	ns
Rise Time		t_r	-	37.1	80	
Turn-Off Delay Time		$t_{d(off)}$	-	12.2	25	
Fall Time		t_f	-	23	50	
Gate Charge	(V_{DS} = 48 Vdc, I_D = 9.0 Adc, V_{GS} = 10 Vdc) (Note 3)	Q_T	-	7.1	15	nC
		Q_1	-	1.7	-	
		Q_2	-	3.5	-	
SOURCE-DRAIN DIODE CHARACTERISTICS						
Forward On-Voltage	(I_S = 9.0 Adc, V_{GS} = 0 Vdc) (Note 3) (I_S = 19 Adc, V_{GS} = 0 Vdc, T_J = 150°C)	V_{SD}	- -	0.98 0.86	1.20 -	Vdc
Reverse Recovery Time	(I_S = 9.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs) (Note 3)	t_{rr}	-	28.9	-	ns
		t_a	-	21.6	-	
		t_b	-	7.3	-	
Reverse Recovery Stored Charge		Q_{RR}	-	0.036	-	μC

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

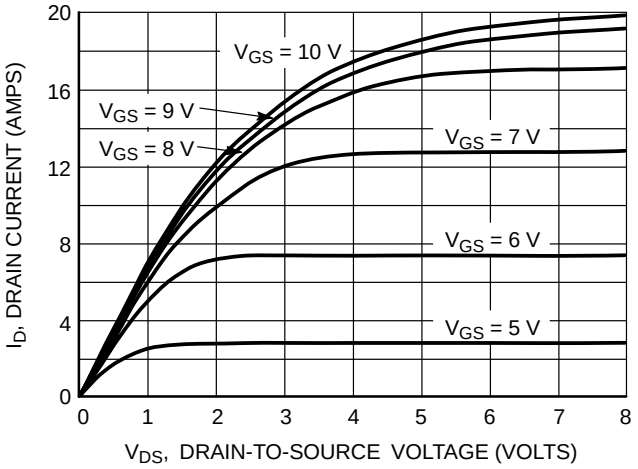


Figure 1. On-Region Characteristics

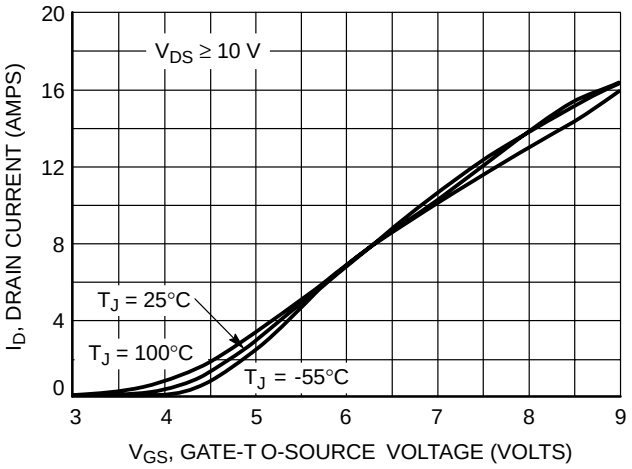


Figure 2. Transfer Characteristics

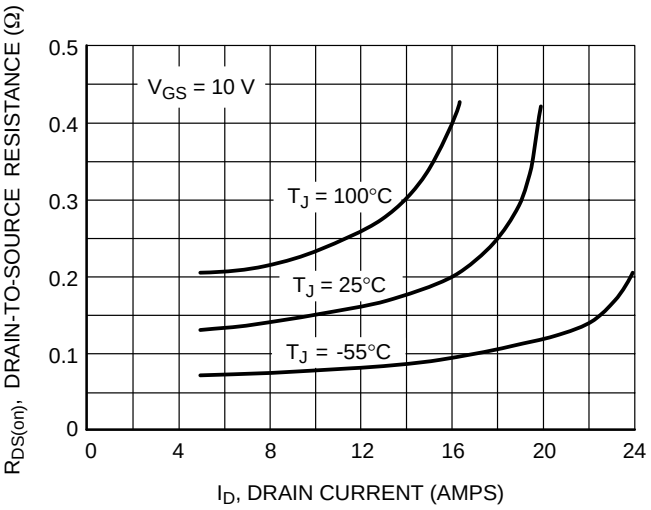


Figure 3. On-Resistance versus Gate-To-Source Voltage

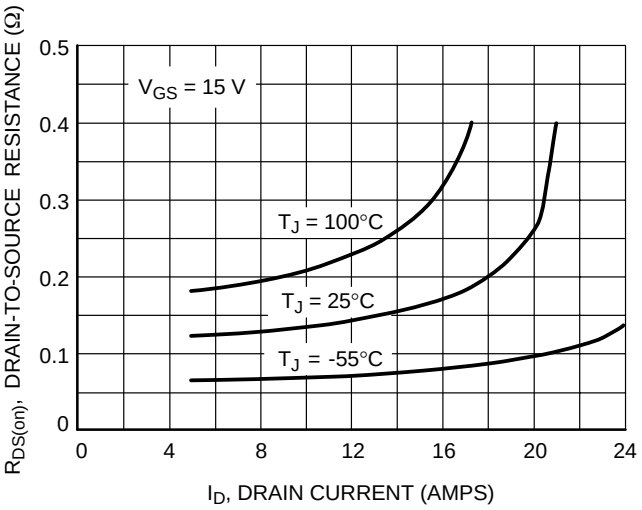


Figure 4. On-Resistance versus Drain Current and Gate Voltage

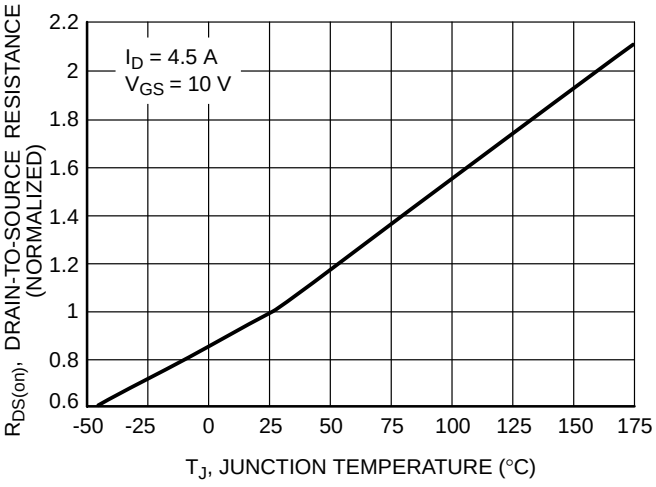


Figure 5. On-Resistance Variation with Temperature

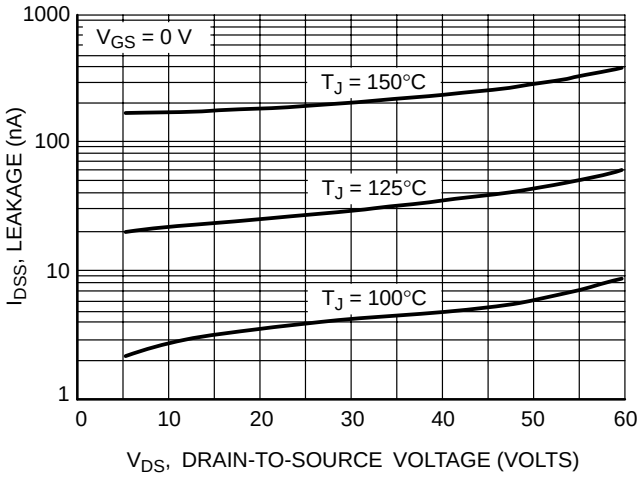


Figure 6. Drain-To-Source Leakage Current versus Voltage

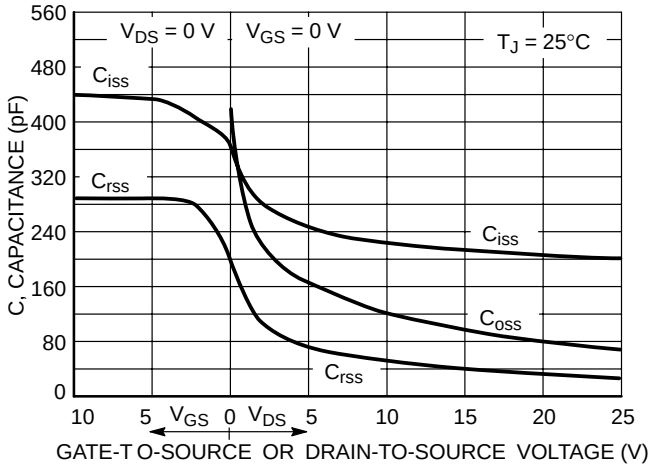


Figure 7. Capacitance Variation

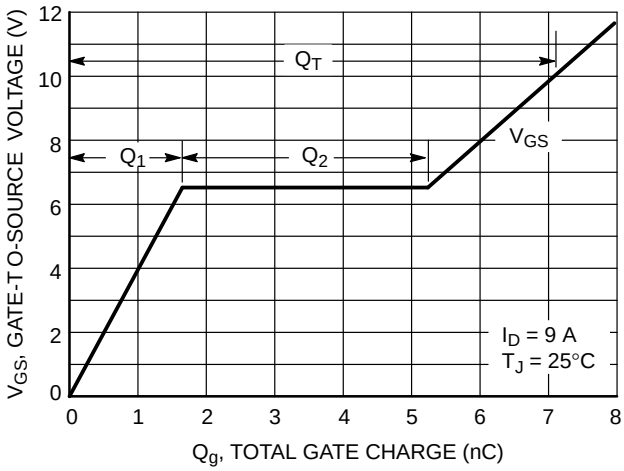


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

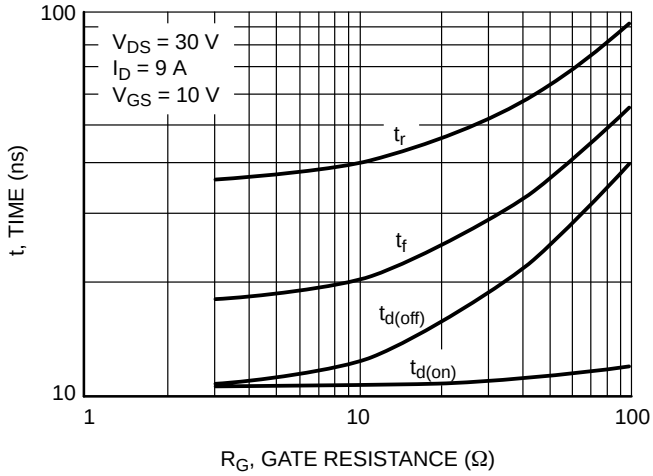


Figure 9. Resistive Switching Time Variation versus Gate Resistance

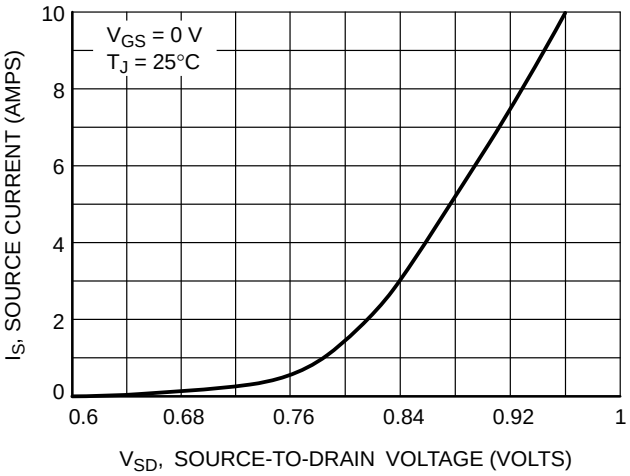


Figure 10. Diode Forward Voltage versus Current

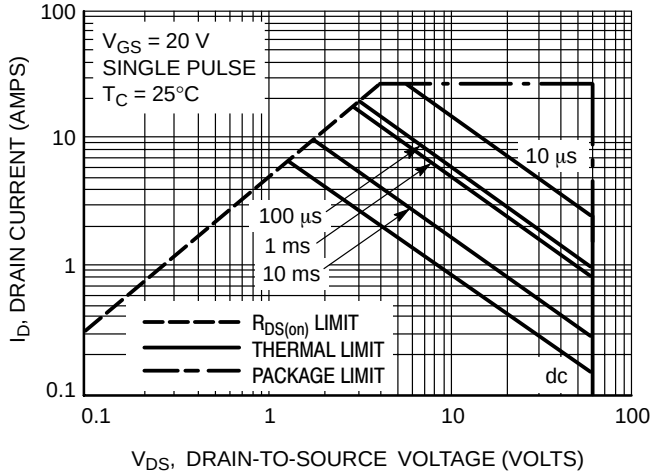


Figure 11. Maximum Rated Forward Biased Safe Operating Area

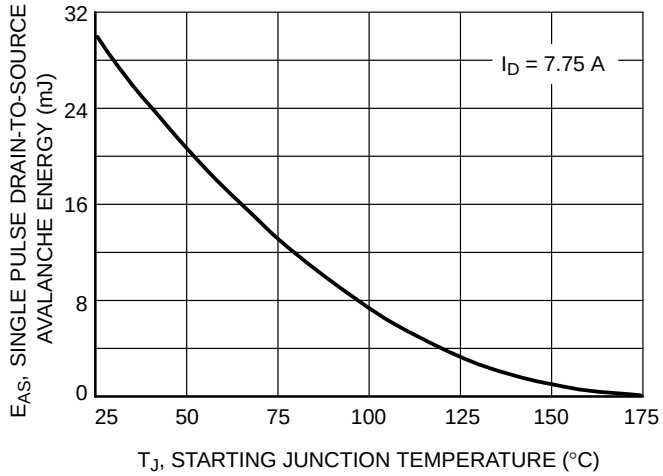


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

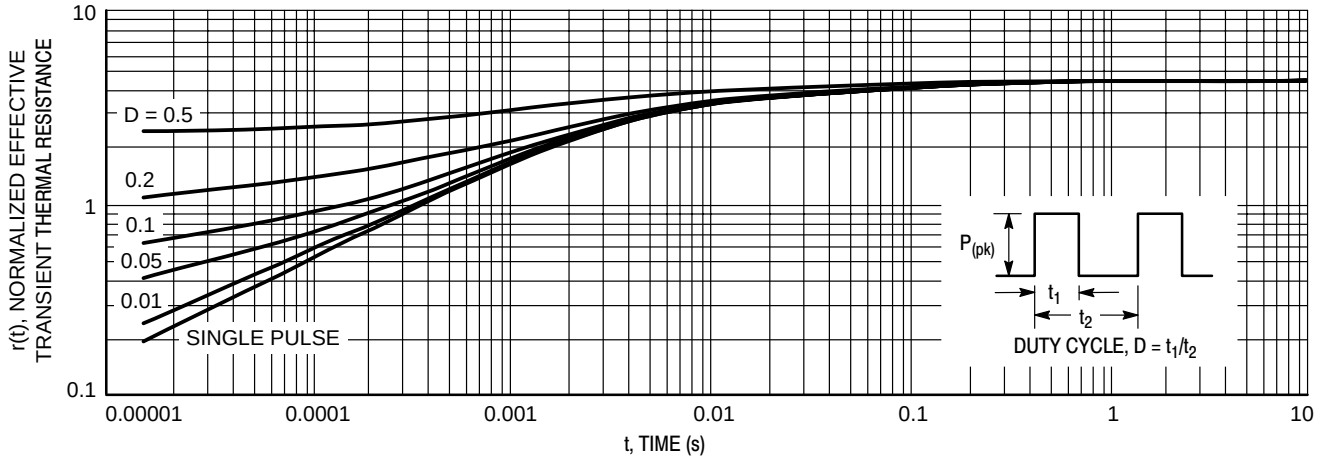
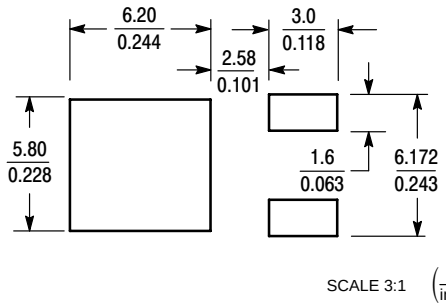


Figure 13. Thermal Response

INFORMATION FOR USING THE DPAK SURFACE MOUNT PACKAGE

RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



POWER DISSIPATION FOR A SURFACE MOUNT DEVICE

The power dissipation for a surface mount device is a function of the drain pad size. These can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, R_{JA}, the thermal resistance from the device junction to ambient, and the operating temperature, T_A. Using the values provided on the data sheet, P_D can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device. For a DPAK device, P_D is calculated as follows.

$$P_D = \frac{175°C - 25°C}{71.4°C/W} = 2.1 \text{ Watts}$$

The 71.4°C/W for the DPAK package assumes the use of 0.5 sq. in. source pad on a glass epoxy printed circuit board to achieve a power dissipation of 2.1 W. There are other alternatives to achieving higher power dissipation from the surface mount packages. One is to increase the area of the drain pad. By increasing the area of the drain pad, the power dissipation can be increased. Although one can almost double the power dissipation with this method, one will be giving up area on the printed circuit board which can defeat the purpose of using surface mount technology. For example, a graph of R_{JA} versus drain pad area is shown in Figure 14.

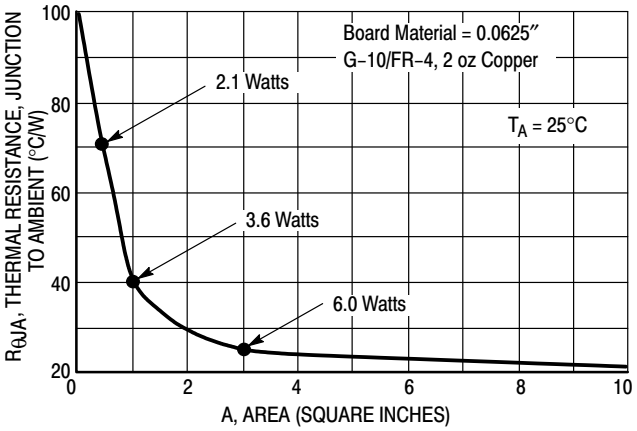
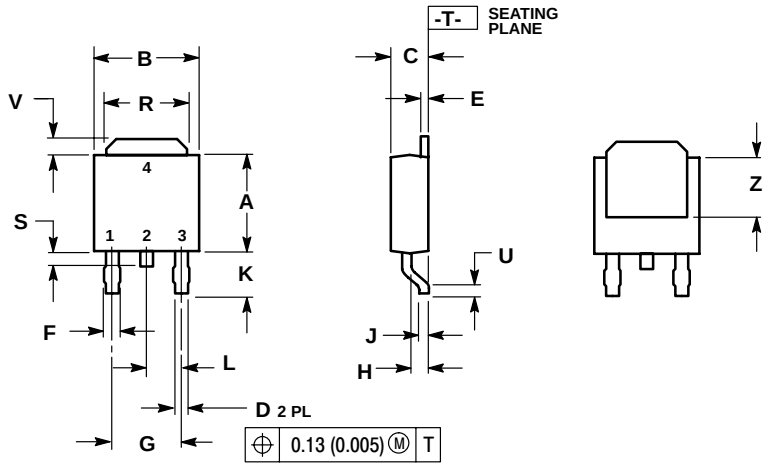


Figure 14. Thermal Resistance versus Drain Pad Area for the DPAK Package (Typical)

PACKAGE DIMENSIONS

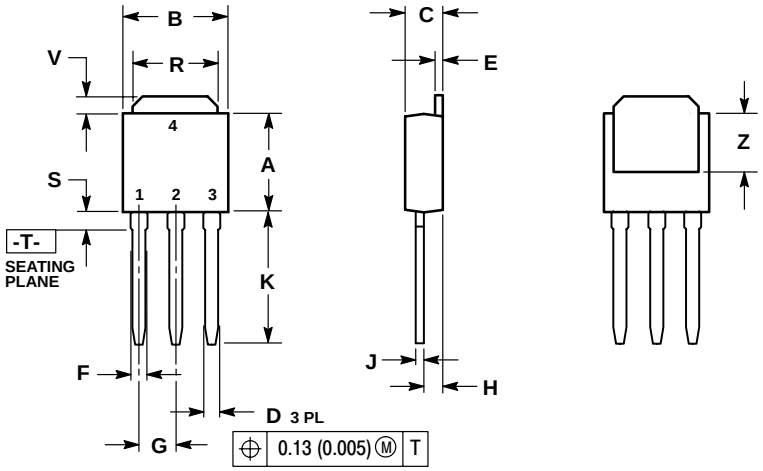
DPAK
CASE 369C-01
ISSUE O



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.025	0.040	0.63	1.01
U	0.020	---	0.51	---
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

DPAK
CASE 369D-01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

PUBLICATION ORDERING INFORMATION

Literature Fulfillment:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: ONlit@hibbertco.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada

JAPAN: ON Semiconductor, Japan Customer Focus Center
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051
Phone: 81-3-5773-3850

ON Semiconductor Website: http://onsemi.com

For additional information, please contact your local
Sales Representative.