Preferred Device

PNP Silicon General Purpose Amplifier Transistor

This PNP Silicon Epitaxial Planar Transistor is designed for general purpose amplifier applications. This device is housed in the SC-70/SOT-323 package which is designed for low power surface mount applications.

- High h_{FE}, 210-460
- Low V_{CE(sat)}, < 0.5 V
- Available in 8 mm, 7-inch/3000 Unit Tape and Reel

MAXIMUM RATINGS $(T_A = 25^{\circ}C)$

Rating	Symbol	Value	Unit
Collector-Base Voltage	$V_{(BR)CBO}$	45	Vdc
Collector–Emitter Voltage	$V_{(BR)CEO}$	45	Vdc
Emitter-Base Voltage	$V_{(BR)EBO}$	7.0	Vdc
Collector Current – Continuous	Ic	100	mAdc
Collector Current – Peak	I _{C(P)}	200	mAdc

THERMAL CHARACTERISTICS

Rating	Symbol	Max	Unit
Power Dissipation (Note 1)	P_{D}	150	mW
Junction Temperature	TJ	150	°C
Storage Temperature Range	T _{stg}	-55 to +150	°C

ELECTRICAL CHARACTERISTICS

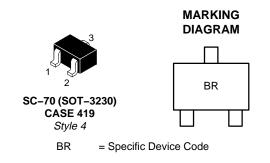
Characteristic	Symbol	Min	Max	Unit
Collector–Emitter Breakdown Voltage $(I_C = 2.0 \text{ mAdc}, I_B = 0)$	V _{(BR)CEO}	45	_	Vdc
Collector–Base Breakdown Voltage ($I_C = 10 \mu Adc, I_E = 0$)	V _{(BR)CBO}	45	_	Vdc
Emitter–Base Breakdown Voltage ($I_E = 10 \mu Adc, I_E = 0$)	V _{(BR)EBO}	7.0	_	Vdc
Collector–Base Cutoff Current $(V_{CB} = 20 \text{ Vdc}, I_E = 0)$	I _{CBO}	_	0.1	μΑ
Collector–Emitter Cutoff Current $(V_{CE} = 10 \text{ Vdc}, I_B = 0)$	I _{CEO}	_	100	μΑ
DC Current Gain (Note 2) (V _{CE} = 10 Vdc, I _C = 2.0 mAdc)	h _{FE1}	210	340	1
Collector–Emitter Saturation Voltage (Note 2) (I _C = 100 mAdc, I _B = 10 mAdc)	V _{CE(sat)}	_	0.5	Vdc

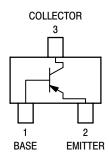
- Device mounted on a FR-4 glass epoxy printed circuit board using the minimum recommended footprint.
- 2. Pulse Test: Pulse Width $\leq 300 \,\mu\text{s}$, D.C. $\leq 2\%$.



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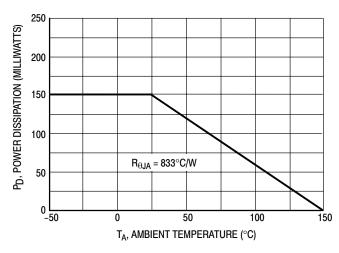


ORDERING INFORMATION

Device	Package	Shipping [†]
MSB1218A-RT1	SC-70	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Preferred devices are recommended choices for future use and best overall value.



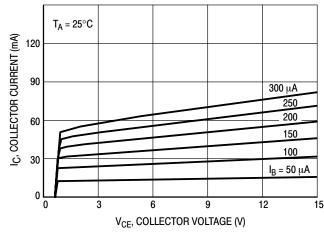
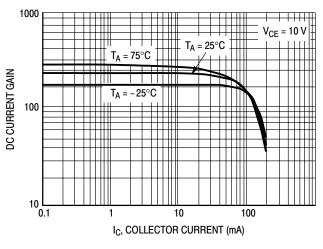


Figure 1. Derating Curve

Figure 2. I_C - V_{CE}



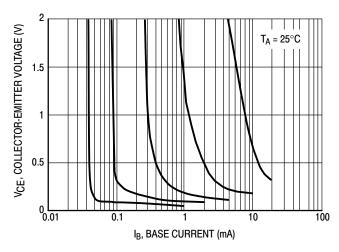


Figure 3. DC Current Gain

Figure 4. Collector Saturation Region

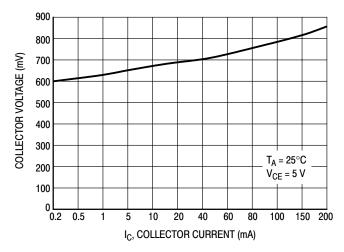
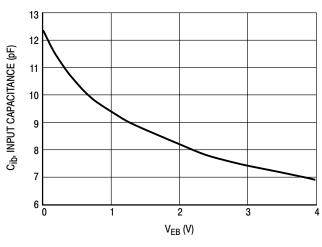


Figure 5. On Voltage



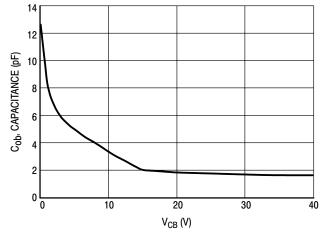
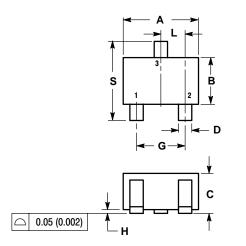


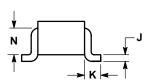
Figure 6. Capacitance

Figure 7. Capacitance

PACKAGE DIMENSIONS

SC-70 (SOT-323) CASE 419-04 ISSUE L





NOTES:

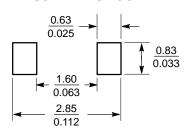
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- 2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIN	IETERS
DIM	MIN	MAX	MIN	MAX
Α	0.071	0.087	1.80	2.20
В	0.045	0.053	1.15	1.35
С	0.032	0.040	0.80	1.00
D	0.012	0.016	0.30	0.40
G	0.047	0.055	1.20	1.40
Н	0.000	0.004	0.00	0.10
J	0.004	0.010	0.10	0.25
K	0.017 REF		0.425 REF	
L	0.026 BSC		0.650 BSC	
N	0.028 REF		0.700 REF	
S	0.079	0.095	2.00	2.40

STYLE 4: PIN 1. CATHODE

2. CATHODE 2. CATHODE 3. ANODE

SOLDERING FOOTPRINT



SCALE 10:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

SOD-323

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