MSB1218A-RT1

Preferred Device

PNP Silicon General Purpose Amplifier Transistor

This PNP Silicon Epitaxial Planar Transistor is designed for general purpose amplifier applications. This device is housed in the SC−70/SOT−323 package which is designed for low power surface mount applications.

- High h_{FE}, 210−460
- Low $V_{CE(sat)}$, < 0.5 V
- Available in 8 mm, 7−inch/3000 Unit Tape and Reel

MAXIMUM RATINGS (T_A = 25°C)

Rating	Symbol	Value	Unit
Collector−Base Voltage	$V_{(BR)CBO}$	45	Vdc
Collector−Emitter Voltage	$V_{(BR)CEO}$	45	Vdc
Emitter−Base Voltage	$V_{(BR)EBO}$	7.0	Vdc
Collector Current − Continuous	I_C	100	mAdc
Collector Current − Peak	$I_{C(P)}$	200	mAdc

THERMAL CHARACTERISTICS

Rating	Symbol	Max	Unit
Power Dissipation (Note 1)	P_D	150	mW
Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
Collector−Emitter Breakdown Voltage (I_C = 2.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	45	−	Vdc
Collector−Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)	$V_{(BR)CBO}$	45	−	Vdc
Emitter−Base Breakdown Voltage (I_E = 10 μAdc, I_E = 0)	$V_{(BR)EBO}$	7.0	−	Vdc
Collector−Base Cutoff Current (V_{CB} = 20 Vdc, I_E = 0)	I_{CBO}	−	0.1	μA
Collector−Emitter Cutoff Current (V_{CE} = 10 Vdc, I_B = 0)	I_{CEO}	−	100	μA
DC Current Gain (Note 2) (V_{CE} = 10 Vdc, I_C = 2.0 mAdc)	h_{FE1}	210	340	−
Collector−Emitter Saturation Voltage (Note 2) (I_C = 100 mAdc, I_B = 10 mAdc)	$V_{CE(sat)}$	−	0.5	Vdc

1. Device mounted on a FR−4 glass epoxy printed circuit board using the minimum recommended footprint.
2. Pulse Test: Pulse Width ≤ 300 μs, D.C. ≤ 2%.

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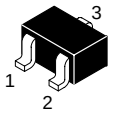
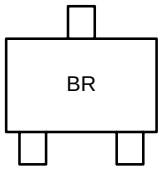
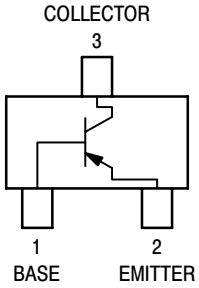


SC−70 (SOT−3230)
CASE 419
Style 4

MARKING DIAGRAM



BR = Specific Device Code



ORDERING INFORMATION

Device	Package	Shipping†
MSB1218A−RT1	SC−70	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Preferred devices are recommended choices for future use and best overall value.

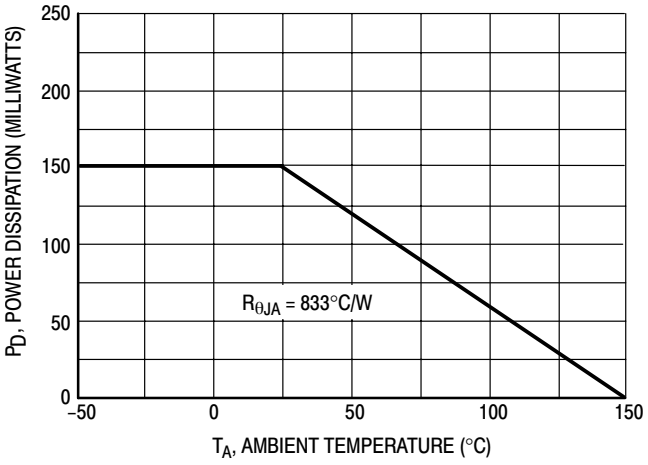


Figure 1. Derating Curve

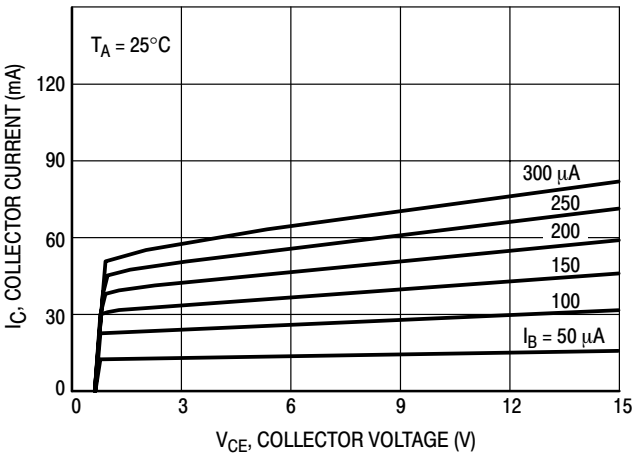


Figure 2. $I_C - V_{CE}$

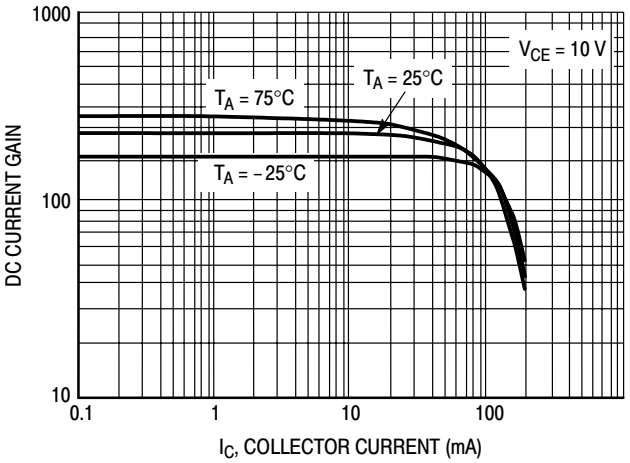


Figure 3. DC Current Gain

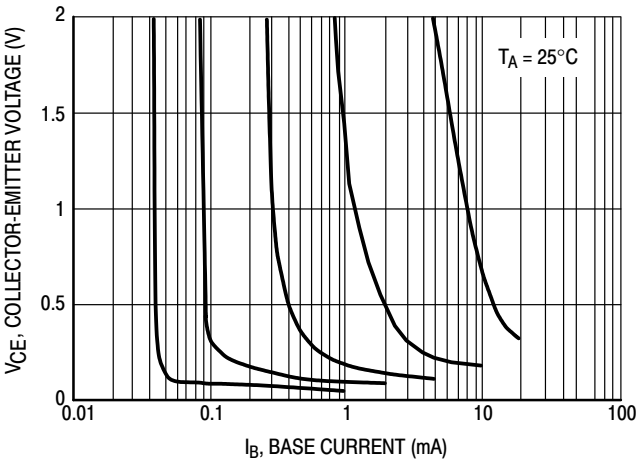


Figure 4. Collector Saturation Region

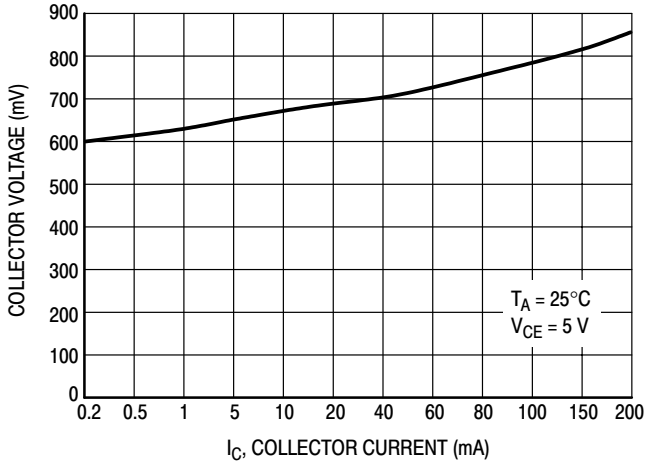


Figure 5. On Voltage

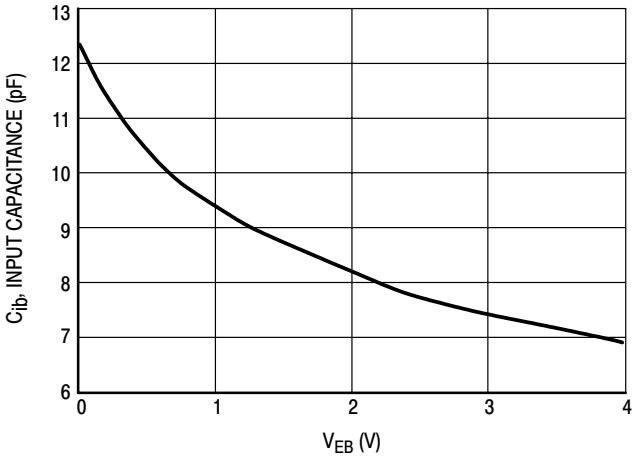


Figure 6. Capacitance

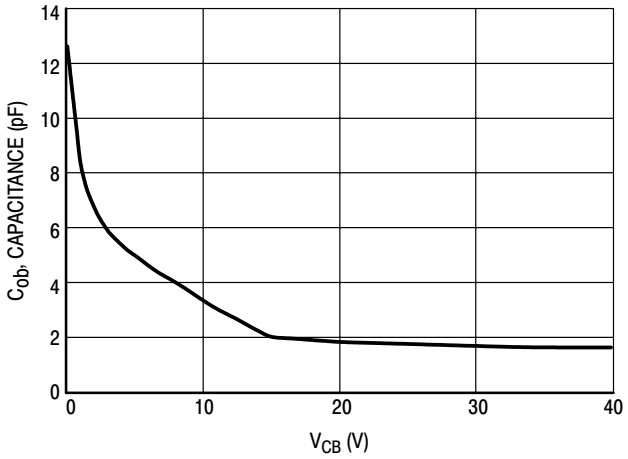
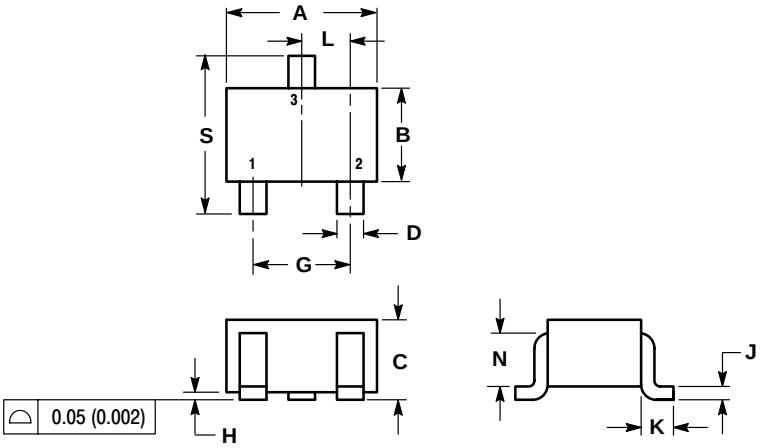


Figure 7. Capacitance

MSB1218A−RT1

PACKAGE DIMENSIONS

SC−70 (SOT−323)
CASE 419−04
ISSUE L

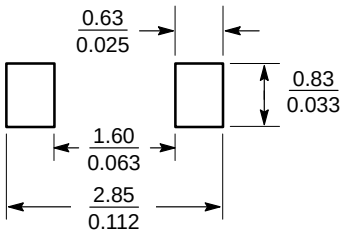


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.032	0.040	0.80	1.00
D	0.012	0.016	0.30	0.40
G	0.047	0.055	1.20	1.40
H	0.000	0.004	0.00	0.10
J	0.004	0.010	0.10	0.25
K	0.017 REF		0.425 REF	
L	0.026 BSC		0.650 BSC	
N	0.028 REF		0.700 REF	
S	0.079	0.095	2.00	2.40

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

SOLDERING FOOTPRINT



SCALE 10:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

SOD−323

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
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For additional information, please contact your local Sales Representative.

MSB1218A−RT1/D