

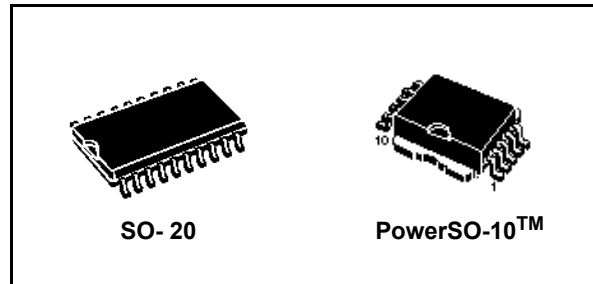
## Quad channel high side driver

### Features

Type	$R_{DS(on)}^{(1)}$	$I_{out}$	$V_{CC}$
VNQ860-E VNQ860SP-E	270 mΩ	0.25 A	36 V

1. Per each channel.

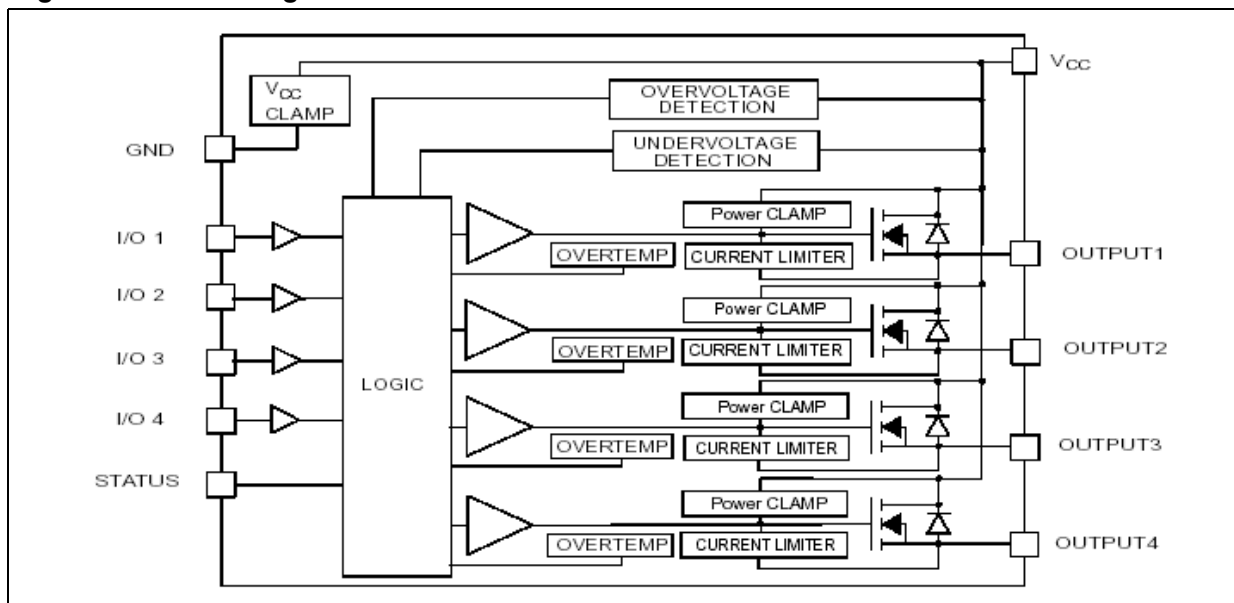
- CMOS compatible I/Os
- Undervoltage and overvoltage shut-down
- Shorted load protection
- Thermal shut-down
- Very low stand-by current
- Protection against loss of ground



### Description

The VNQ860-E, VNQ860SP-E are monolithic devices made using STMicroelectronics VIPower M0-3 technology, intended for driving any kind load with one side connected to ground. Active current limitation combined with thermal shut-down and automatic restart protect the device against overload. Device automatically turns OFF in case of ground pin disconnection. This device is especially suitable for industrial applications in norms conformity with IEC 61131, (Programmable controllers international standard).

Figure 1. Block diagram



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# 1 Maximum rating

**Table 1. Absolute maximum rating**

Symbol	Parameter	Value		Unit
		SO-20	PowerSO-10	
$V_{CC}$	DC supply voltage	41		V
$-V_{CC}$	Reverse DC supply voltage	-0.3		V
$-I_{GND}$	DC reverse ground pin	-200		mA
$I_{OUT}$	DC output current	Internally limited		A
$-I_{OUT}$	Reverse DC output current	-2		A
$I_{IN}$	DC input current	$\pm 10$		mA
$V_{IN}$	Input voltage range	$-3/+V_{CC}$		V
$I_{STAT}$	DC status voltage	$+ V_{CC}$		V
$V_{ESD}$	Electrostatic discharge (R = 1.5 kW; C = 100 pF)	2000		V
$P_{tot}$	Power dissipation at $T_c \leq 25\text{ }^\circ\text{C}$	16	90	W
$T_J$	Junction operating temperature	Internally limited		$^\circ\text{C}$
$T_c$	Case operating temperature	-40 to 150		$^\circ\text{C}$
$T_{stg}$	Storage temperature	-55 to 150		$^\circ\text{C}$

**Table 2. Thermal data**

Symbol	Parameter		Value		Unit
			SO-20	PowerSO-10	
$R_{thJP}$	Thermal resistance junction-pins	Max	8	-	$^\circ\text{C}/\text{W}$
$R_{thJA}$	Thermal resistance junction-ambient	Max	58	52 <sup>(1)</sup>	$^\circ\text{C}/\text{W}$
				37 <sup>(2)</sup>	
$R_{thJC}$	Thermal resistance junction-case	Max	-	1.4	$^\circ\text{C}/\text{W}$

- When mounted on FR4 printed circuit board with 0.5 cm<sup>2</sup> of copper area ( at least 35 $\mu$  thick ) connected to all  $V_{CC}$  pins.
- When mounted on FR4 printed circuit board with 6 cm<sup>2</sup> of copper area ( at least 35 $\mu$  thick ) connected to all  $V_{CC}$  pins.

## 2 Pin connection

Figure 2. Configuration diagram (top view) and suggested connections for unused and n.c. pins

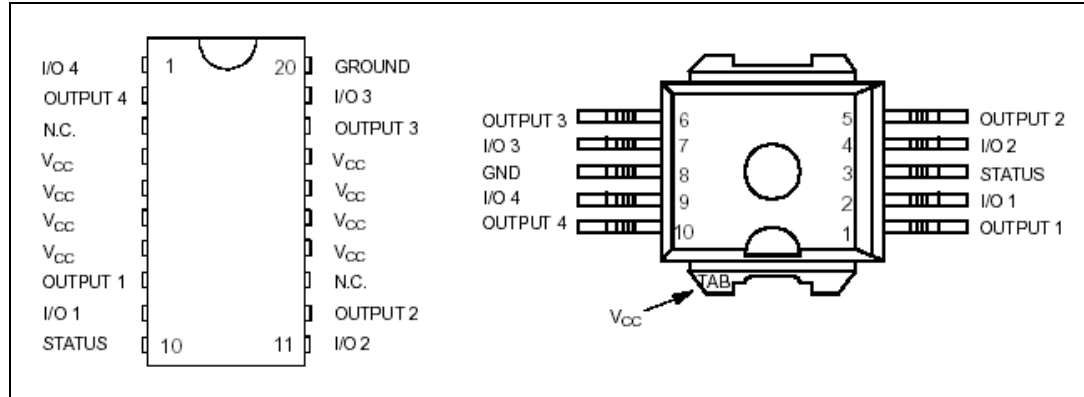
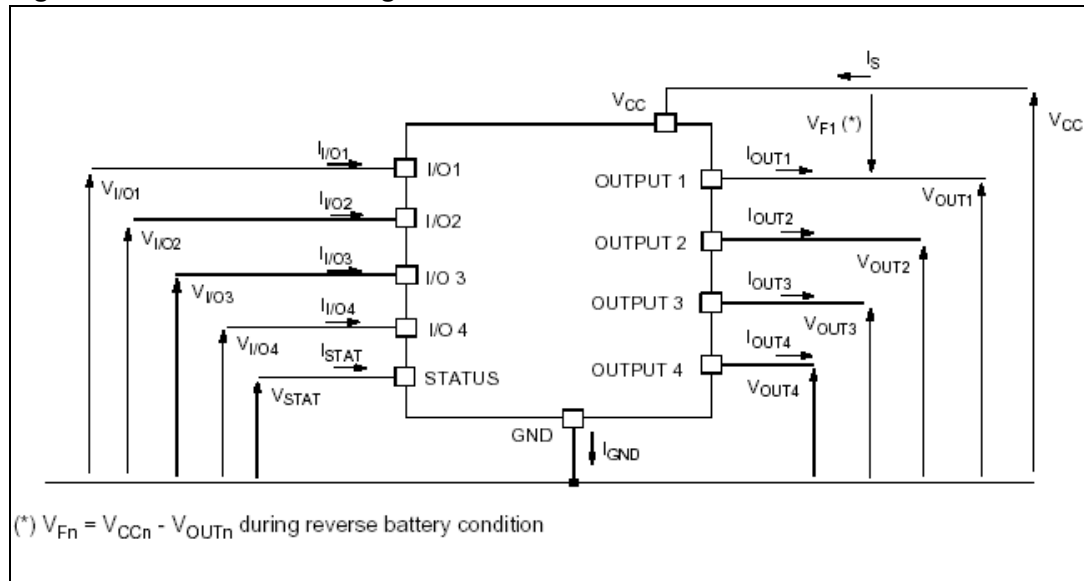


Table 3. Pin connection

Connection / pin	Status	N.C.	Output	Input
Floating	X	X	X	X
To ground		X		Through 10 kΩ resistor

Figure 3. Current and voltage conventions



### 3 Electrical characteristics

(8 V < V<sub>CC</sub> < 36 V; -40 °C < T<sub>J</sub> < 150 °C; unless otherwise specified)

**Table 4. Power section**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V <sub>CC</sub>	Operating supply voltage		5.5		36	V
V <sub>USD</sub>	Undervoltage shut-down		3	4	5.5	V
V <sub>OV</sub>	Overvoltage shut-down		36	42	48	V
R <sub>ON</sub>	On state resistance (per channel)	I <sub>OUT</sub> = 0.25 A; T <sub>J</sub> = 25 °C; I <sub>OUT</sub> = 0.25 A;			270 540	mΩ
I <sub>S</sub>	Supply current	OFF state; V <sub>CC</sub> = 24 V; T <sub>C</sub> = 25 °C ON state ( all channels ON )		70 5	120 10	μA mA
I <sub>LGND</sub>	Output current	V <sub>CC</sub> - V <sub>STAT</sub> = V <sub>IN</sub> = V <sub>GND</sub> = 24 V; V <sub>OUT</sub> = 0 V			1	mA
I <sub>L(OFF)</sub>	OFF state output current	V <sub>IN</sub> = V <sub>OUT</sub> = 0 V	0		10	μA
I <sub>OUTleak</sub>	OFF state output leakage current	V <sub>IN</sub> = V <sub>GND</sub> = 0 V; V <sub>CC</sub> = V <sub>OUT</sub> = 24 V; T <sub>A</sub> = 25 °C			240	μA
I <sub>OUTleak</sub>	OFF state output leakage current	V <sub>IN</sub> = V <sub>GND</sub> = 0 V; V <sub>CC</sub> = 24 V; V <sub>OUT</sub> = 10 V; T <sub>A</sub> = 25 °C			100	μA

**Table 5. Switching ( V<sub>CC</sub> = 24 V)**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
t <sub>(ON)</sub>	Turn-on delay time of Output current	R <sub>L</sub> = 96 from V <sub>IN</sub> rising edge to V <sub>OUT</sub> = 2.4 V		10		μs
t <sub>(OFF)</sub>	Turn-off delay time of Output current	R <sub>L</sub> = 96 from V <sub>IN</sub> rising edge to V <sub>OUT</sub> = 21.6 V		40		μs
(dV <sub>OUT</sub> /dt) <sub>on</sub>	Turn-on voltage slope	R <sub>L</sub> = 96 from V <sub>OUT</sub> = 2.4 V to 19.2 V		0.75		V/μs
(dV <sub>OUT</sub> /dt) <sub>off</sub>	Turn-off voltage slope	R <sub>L</sub> = 96 from V <sub>OUT</sub> = 21.6 V to 2.4 V		0.25		V/μs

**Table 6. Protections (per channel)**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$I_{lim}$	Current limitation		0.35	0.7	1.1	A
$T_{(hyst)}$	Thermal hysteresis		7	15		°C
$T_{TSD}$	Thermal shut-down temperature		150	175	200	°C
$T_R$	Reset temperature		135			°C
$V_{demag}$	Turn-off output clamp voltage	$I_{OUT} = 0.25 \text{ A}, V_{CC} = 24 \text{ V}$	$V_{CC} - 59$	$V_{CC} - 52$	$V_{CC} - 47$	V

**Table 7. Logical input (per channel)**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$V_{IL}$	Low level input voltage				1.25	V
$I_{IL}$	Low level input current	$V_{IN} = 1.25 \text{ V}$	1			$\mu\text{A}$
$V_{IH}$	High level input voltage		3.25			V
$I_{IH}$	High level input current	$V_{IN} = 3.25 \text{ V}$			10	$\mu\text{A}$
$V_{I(HYST)}$	Input hysteresis voltage		0.5			V
$I_{IN}$	Input current	$V_{IN} = V_{CC} = 36 \text{ V}$			200	$\mu\text{A}$
$V_{OL}$	I/O output voltage	$I_{IN} = 5 \text{ mA}$ ( Fault condition )			1	V

**Table 8. Status pin**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$V_{STAT}$	Status low output voltage	$I_{STAT} = 5 \text{ mA}$ ( Fault condition )			1	V
$I_{LSTAT}$	Status leakage current	Normal operation; $V_{STAT} = V_{CC} = 36 \text{ V}$			10	$\mu\text{A}$
$C_{STAT}$	Status pin input capacitance	Normal operation; $V_{STAT} = 5 \text{ V}$			100	pF

**Table 9.  $V_{CC}$  - output diode**

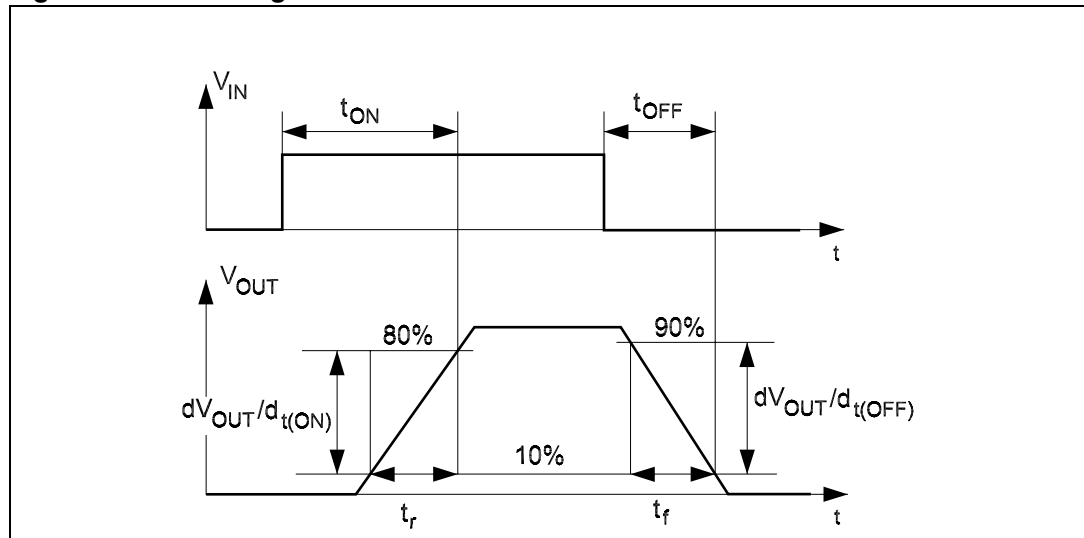
Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$V_F$	Forwardon voltage	$-I_{OUT} = 0.3 \text{ A}; T_J = 150 \text{ °C}$			1	V

## 4 Truth table and switching characteristics

Table 10. Truth table

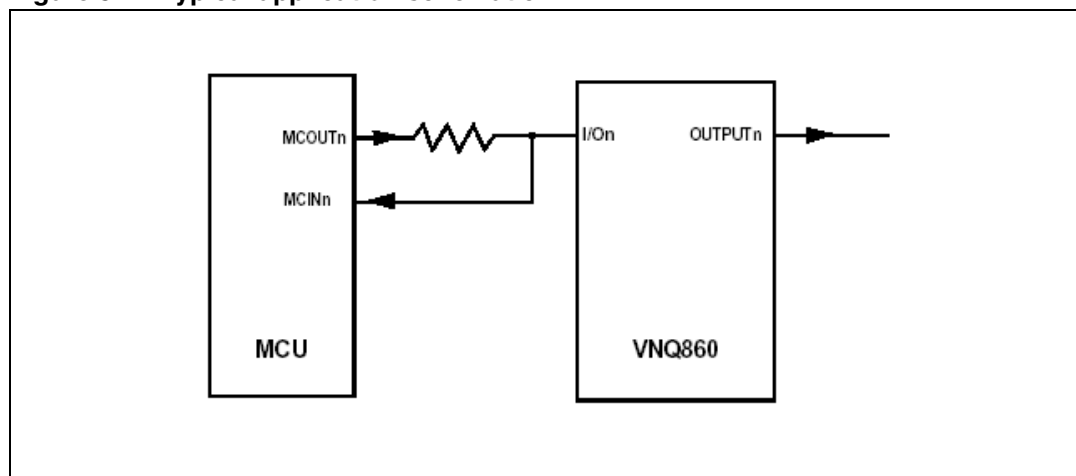
Conditions	MCOUTn	I/On	OUTPUTn	STATUS
Normal operation	L	L	L	H
	H	H	H	H
Current limitation	L	L	L	H
	H	H	X	H
Overtemperature	L	L	L	X
	H	Driven low	L	X
Undervoltage	L	L	L	X
	H	H	L	X
Overvoltage	L	L	L	H
	H	H	L	H

Figure 4. Switching characteristics



## 5 Typical application schematic

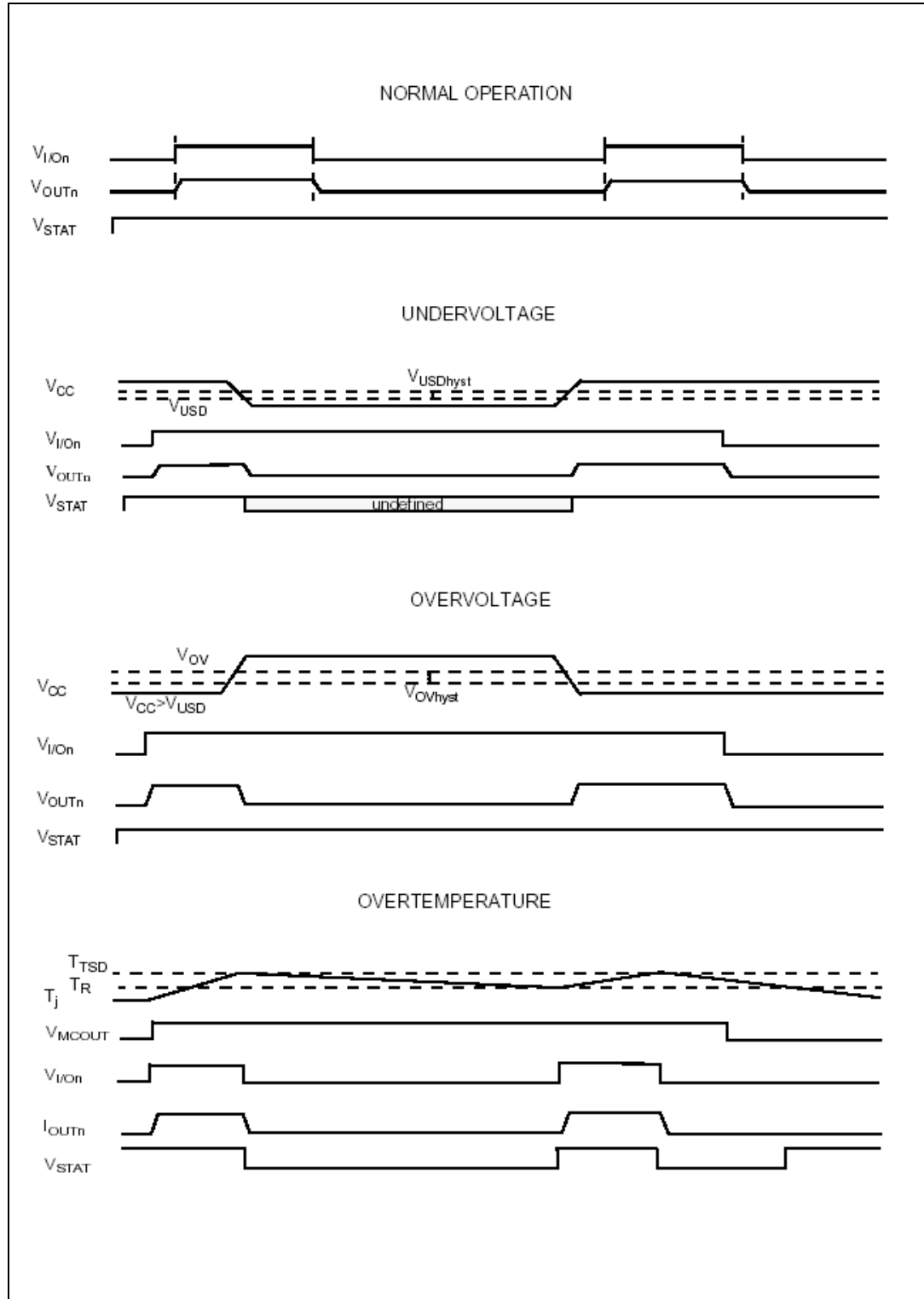
Figure 5. Typical application schematic





# 6 Waveforms

Figure 6. Waveforms



# 7 PowerSO-10™ thermal data

Figure 7. PowerSO-10™ PC board

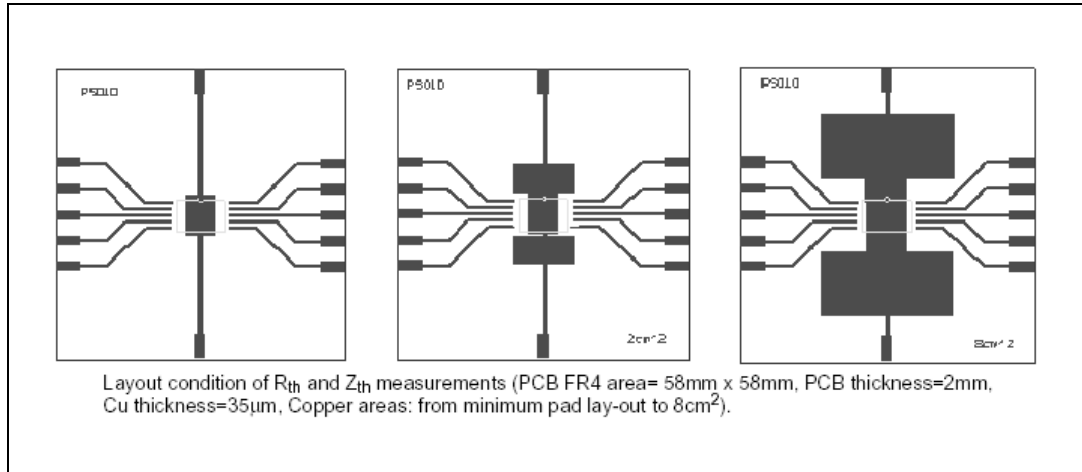
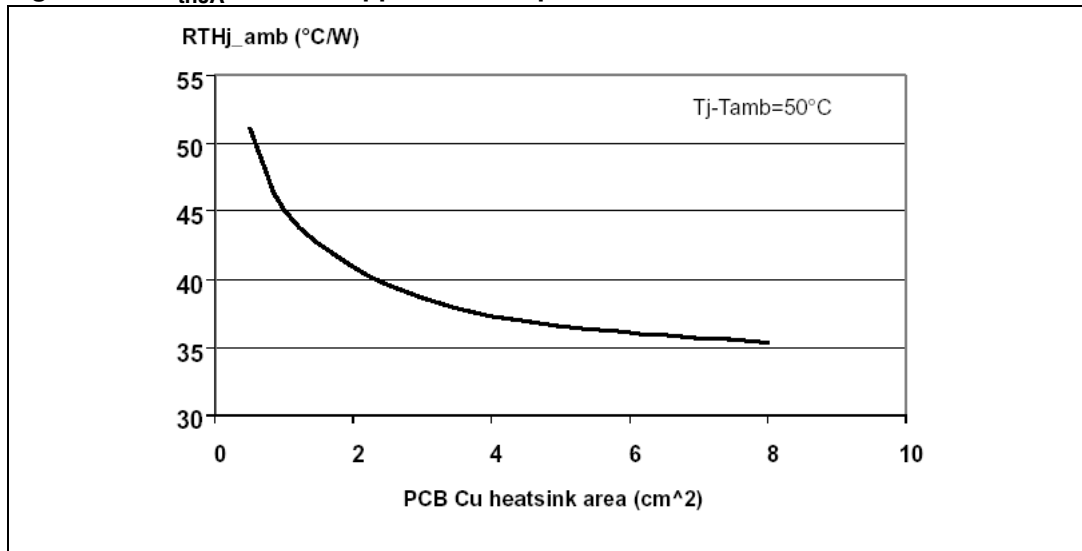


Figure 8.  $R_{thJA}$  vs PBC copper area in open box free air condition



## 8 Reverse polarity protection

A schematic solution to protect the IC against a reverse polarity condition is proposed.

This schematic is effective with any type of load connected to the outputs of the IC.

The  $R_{GND}$  resistor value can be selected according to the following conditions to be met:

1.  $R_{GND} \leq 600 \text{ mV} / (I_S \text{ in ON state max})$ .
2.  $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where  $-I_{GND}$  is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

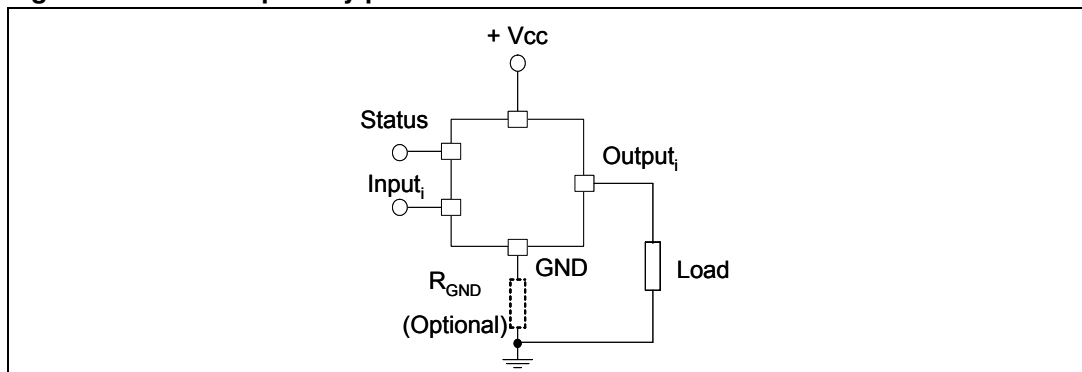
The power dissipation associated to  $R_{GND}$  during reverse polarity condition is:

$$PD = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared by several different ICs. In such case  $I_S$  value on formula (1) is the sum of the maximum ON-state currents of the different devices.

Please note that if the microprocessor ground and the device ground are separated then the voltage drop across the  $R_{GND}$  (given by  $I_S$  in ON state max \*  $R_{GND}$ ) produce a difference between the generated input level and the IC input signal level. This voltage drop will vary depending on how many devices are ON in the case of several high side switches sharing the same  $R_{GND}$ .

**Figure 9. Reverse polarity protection**



## 9 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com).

**Table 11. PowerSO-10™ mechanical data**

Dim.	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	3.35		3.65	0.132		0.144
A1	0.00		0.10	0.000		0.004
B	0.40		0.60	0.016		0.024
c	0.35		0.55	0.013		0.022
D	9.40		9.60	0.370		0.378
D1	7.40		7.60	0.291		0.300
E	9.30		9.50	0.366		0.374
E1	7.20		7.40	0.283		0.291
E2	7.20		7.60	0.283		0.300
E3	6.10		6.35	0.240		0.250
E4	5.90		6.10	0.232		0.240
e		1.27			0.050	
F	1.25		1.35	0.049		0.053
H	13.80		14.40	0.543		0.567
h		0.50			0.002	
L	1.20		1.80	0.047		0.071
q		1.70			0.067	
a	0°		8°			

Figure 10. PowerSO-10™ package dimensions

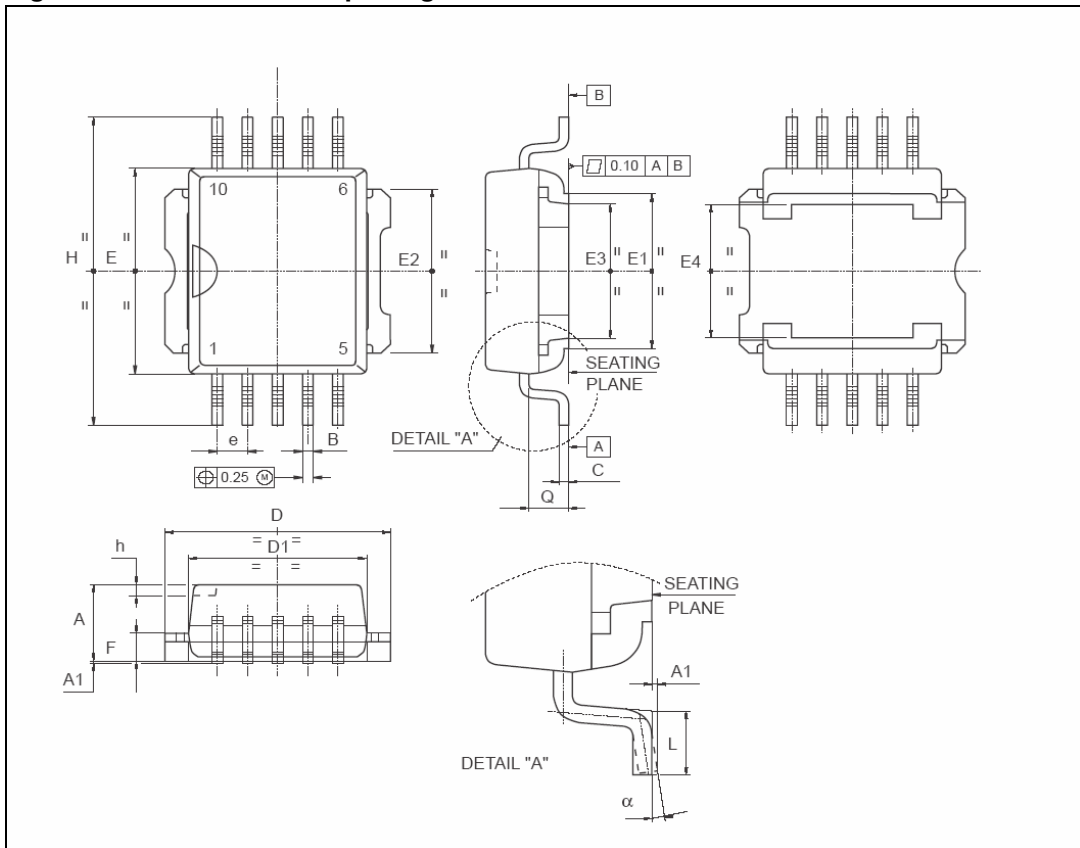


Figure 11. PowerSO-10™ suggested pad and tube shipment (no suffix)

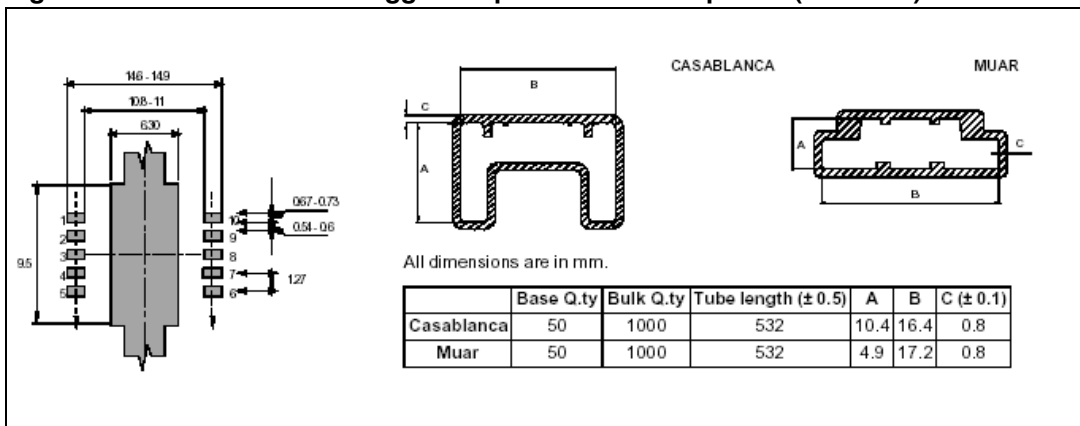


Figure 12. Tape and reel shipment (suffix “TR”)

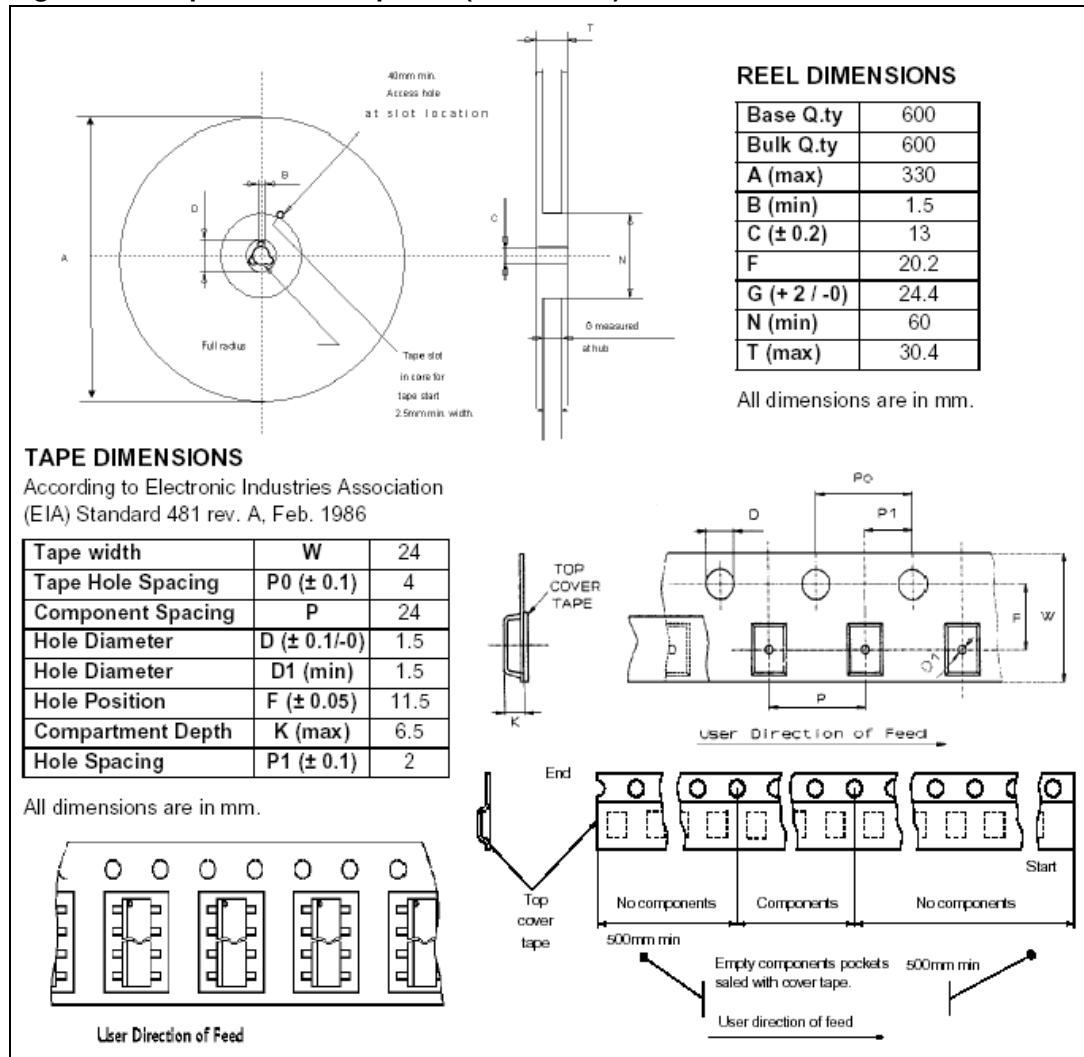


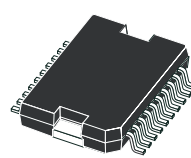
Figure 13. PowerSO-20 mechanical data and package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.6			0.142
a1	0.1		0.3	0.004		0.012
a2			3.3			0.130
a3	0		0.1	0.000		0.004
b	0.4		0.53	0.016		0.021
c	0.23		0.32	0.009		0.013
D (1)	15.8		16	0.622		0.630
D1 (2)	9.4		9.8	0.370		0.386
E	13.9		14.5	0.547		0.570
e		1.27			0.050	
e3		11.43			0.450	
E1 (1)	10.9		11.1	0.429		0.437
E2			2.9			0.114
E3	5.8		6.2	0.228		0.244
G	0		0.1	0.000		0.004
H	15.5		15.9	0.610		0.626
h			1.1			0.043
L	0.8		1.1	0.031		0.043
N	8*(typ.)					
S	8*(max.)					
T		10			0.394	

(1) "D and E1" do not include mold flash or protrusions.  
 - Mold flash or protrusions shall not exceed 0.15mm (0.006")  
 - Critical dimensions: "E", "G" and "a3".  
 (2) For subcontractors, the limit is the one quoted in jecdec MO-166

**OUTLINE AND MECHANICAL DATA**

Weight: 1.9gr



**JEDEC MO-166**

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**PowerSO-20**

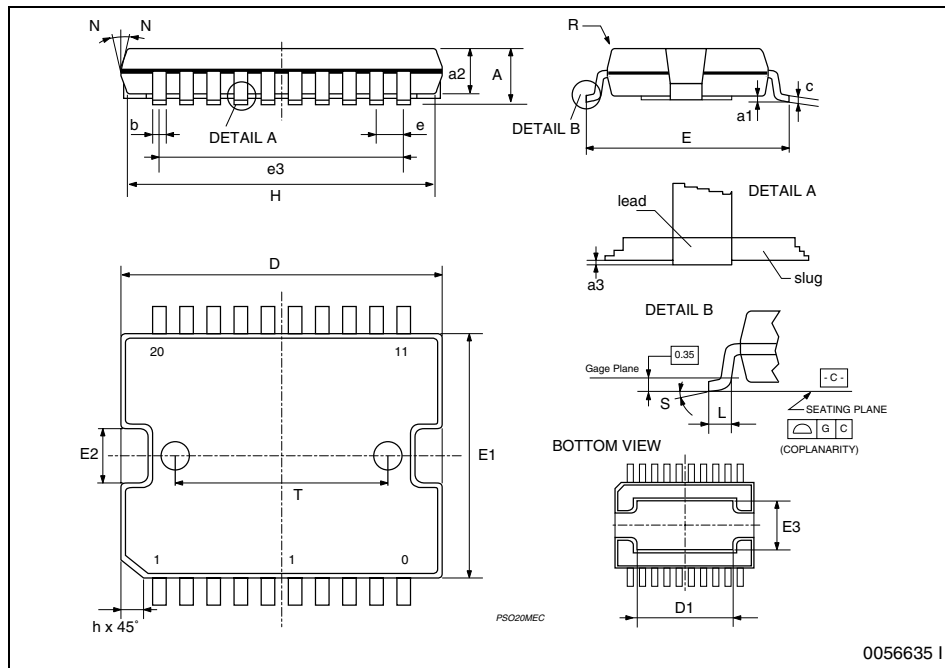


Figure 14. SO-20 tube shipment ( no suffix )

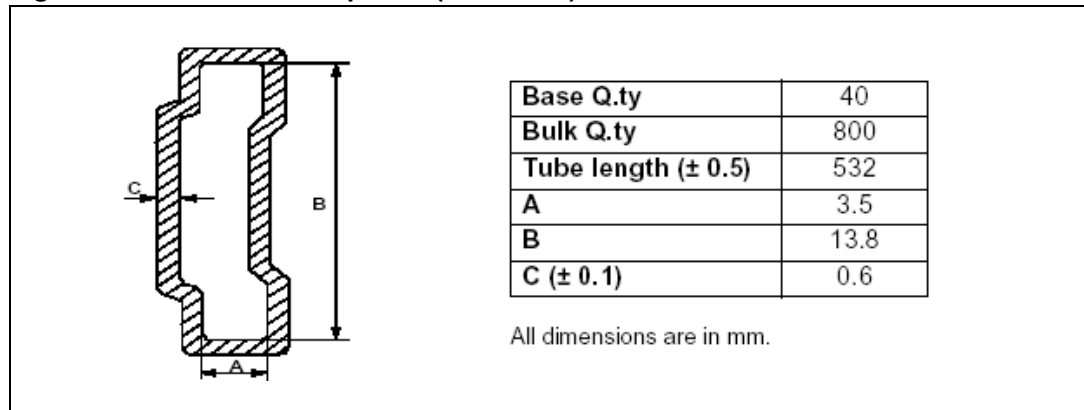
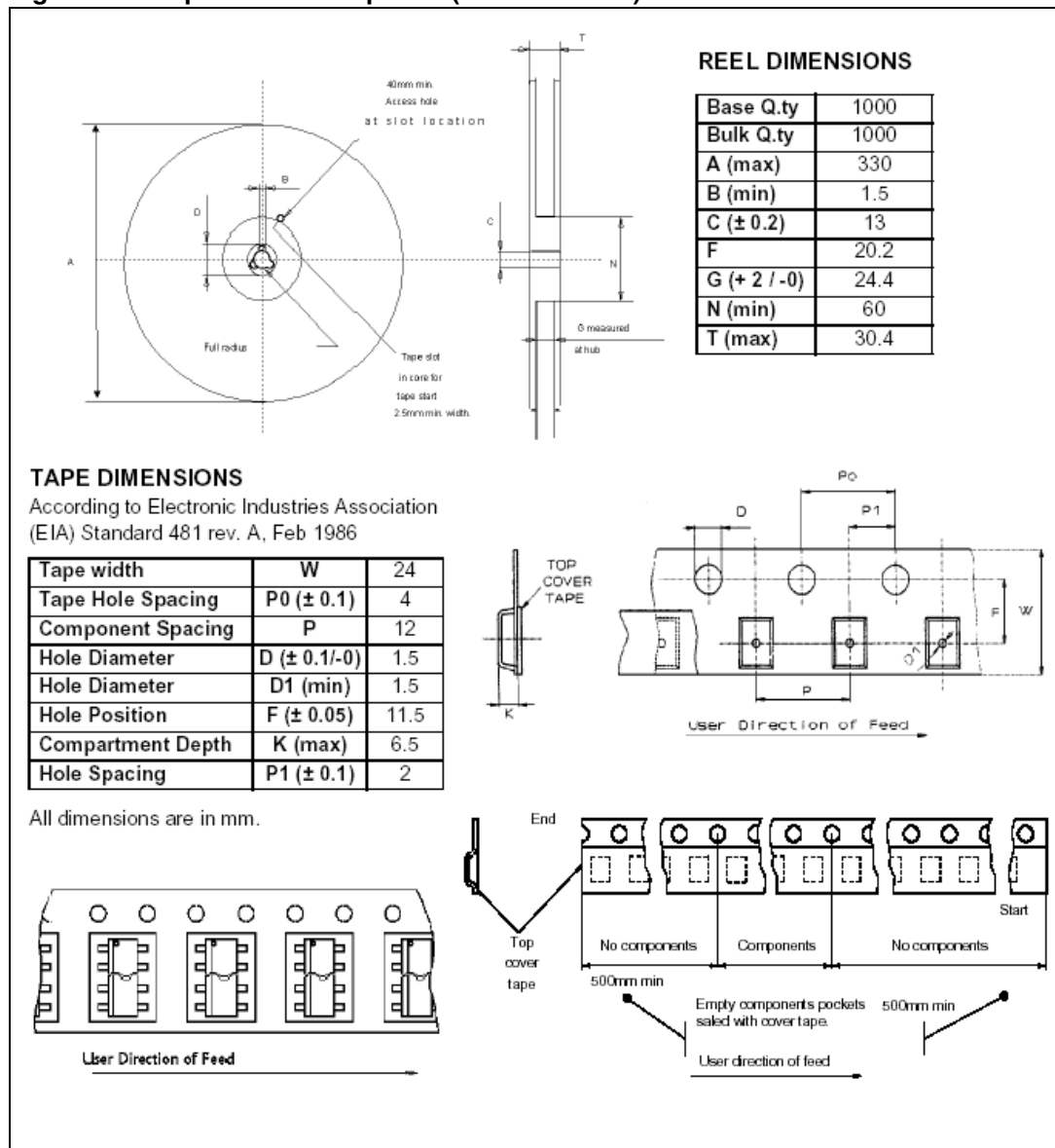


Figure 15. Tape and reel shipment ( suffix “13TR“)





## 10 Order codes

**Table 12. Order codes**

Order codes	Package	Packaging
VNQ860	SO-20	Tube
VNQ860SP	PowerSO-10™	
VNQ86013TR-E	SO-20	Tape and reel
VNQ860SP13TR-E	PowerSO-10™	

## 11 Revision history

**Table 13. Document revision history**

Date	Revision	Changes
14-Jul-2005	1	Updates , new template
7-Nov-2005	2	Few updates
07-Jul-2008	3	Added <a href="#">Section 8 on page 11</a>

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