PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 Rev. A1/A2/A3 Silicon Errata

The PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 (Rev. A1/A2/A3) devices you have received were found to conform to the specifications and functionality described in the following documents:

- DS70293 – "*PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 Data Sheet*"
- DS70157 – "*dsPIC30F/33F Programmer's Reference Manual*"

The exceptions to the specifications in the documents listed above are described in this section. The specific devices for which these exceptions are described are listed below:

- PIC24HJ128GP504
- PIC24HJ128GP502
- PIC24HJ128GP204
- PIC24HJ128GP202
- PIC24HJ64GP504
- PIC24HJ64GP502
- PIC24HJ64GP204
- PIC24HJ64GP202
- PIC24HJ32GP304
- PIC24HJ32GP302

PIC24HJ32GP302/304, PIC24HJ64GPX02/X04 and PIC24HJ128GPX02/X04 Rev. A1/A2/A3 silicon is identified by performing a "Reset and Connect" operation to the device using MPLAB® ICD 2 with MPLAB IDE v7.40 or later. The output window will show a successful connection to the device specified in *Configure>Select Device*. The resulting DEVREV register values for Rev. A1/A2/A3 silicon are 0x3001, 0x3002 and 0x3003, respectively.

The errata described in this document will be addressed in future revisions of silicon.

Silicon Errata Summary

The following list summarizes the errata described in further detail in the remainder of this document:

1. UART Module

   The 16x baud clock signal on the BCLK pin is present only when the module is transmitting.

2. UART Module

   When the UART is in 4x mode (BRGH = 1) and using two Stop bits (STSEL = 1), it may sample the first Stop bit instead of the second one.

3. SPI Module

   The SPI transmit buffer full (SPITBF) flag does not get set immediately after writing to the buffer.

4. SPI Module in Frame Master Mode

   The SPI module will generate incorrect frame synchronization pulses in Frame Master mode if FRMDLY = 1.

5. I^2C™ Module

   The BCL bit in I2CSTAT can only be cleared with Word instructions, and can be corrupted with byte instructions and bit operations.

6. I^2C Module

   The ACKSTAT bit is cleared shortly after being set following a slave transmit.

7. I^2C Module: 10-bit Addressing Mode

   When the I^2C module is configured for 10-bit addressing using the same address bits (A10 and A9) as other I^2C devices, A10 and A9 bits may not work as expected.

8. I^2C Module: 10-bit Addressing Mode

   When the I^2C module is configured as a 10-bit slave with an address of 0x102, the I2CxRCV register content for the lower address byte is 0x01 rather than 0x02.

9. I^2C Module

   With the I^2C module enabled, the PORT bits and external Interrupt Input functions (if any) associated with SCL and SDA pins will not reflect the actual digital logic levels on the pins.

10. I^2C Module: 10-bit Addressing Mode

    The 10-bit slave does not set the RBF flag or load the I2CxRCV register, on address match if the Least Significant bits (LSbs) of the address are the same as the 7-bit reserved addresses.

11. UART (UxE Interrupt)

    The UART error interrupt may not occur, or may occur at an incorrect time, if multiple errors occur during a short period of time.

12. UART Module

    When the UART module is operating in 8-bit mode (PDSEL = 0x) and using the IrDA® encoder/decoder (IREN = 1), the module incorrectly transmits a data payload of 80h as 00h.

13. Comparator Module

    When CMCON<CxOUTEN> is set, the Comparator output pin cannot be used as a General Purpose I/O pins even if the Comparator is disabled.

14. Internal Voltage Regulator

    When the VREGS (RCON<8>) bit is set to a logic '0' higher sleep current may be observed.

15. Product Identification

    Revision A2 devices marked as extended temperature range (E) devices, support only industrial temperature range (I).

16. PSV Operations

    An address error trap occurs in certain addressing modes when accessing the first four bytes of any PSV page.

17. ECAN Module

    The ECAN module may not store received data in the correct location.

18. ECAN Module

    The ECAN module does not generate a CAN event interrupt when coming out of Disable mode on bus wake-up activity even if the WAKIE bit in the CiINTE register is set.

The following sections describe the errata and work around to these errata, where they may apply.

1. Module: UART

When the UART is configured for IR interface operations (UxMODE<9:8> = 11), the 16x baud clock signal on the BCLK pin is present only when the module is transmitting. The pin is idle at all other times.

Work around

Configure one of the output compare modules to generate the required baud clock signal when the UART is receiving data or in an Idle state.

2. Module: UART

When the UART is in 4x mode (BRGH = 1) and using two Stop bits (STSEL = 1), it may sample the first Stop bit instead of the second one.

This issue does not affect the other UART configurations.

Work around

Use the 16x baud rate option (BRGH = 0) and adjust the baud rate accordingly.

3. Module: SPI

The SPI transmit buffer full (SPITBF) flag does not get set immediately after writing to the buffer.

Work around

After a write to the SPI buffer, poll the SPITBF flag until the flag gets set, indicating that the transmit buffer is not full. Afterwards, poll the SPITBF flag again until the flag gets cleared, indicating that the transmit has started and that the transmit buffer is empty and another write can occur.

4. Module: SPI

The SPI module will generate incorrect frame synchronization pulses when configured in Frame Master mode if the start of data is selected to coincide with the start of the frame synchronization pulse (FRMEN = 1, SPIFSD = 0, FRMDLY = 1). However, the module functions correctly in Frame Slave mode, and also in Frame Master mode if FRMDLY = 0.

Work around

If DMA is not being used, manually drive the SSx pin (x = 1 or 2) high using the associated PORT register, and then drive it low after the required 1 bit time pulse-width. This operation needs to be performed when the transmit buffer is written.

If DMA is being used, and if no other peripheral modules are using DMA transfers, use a timer interrupt to periodically generate the frame synchronization pulse (using the method described above) after every 8 or 16-bit periods (depending on the data word size, configured using the MODE16 bit).

If FRMDLY = 0, no work around is needed.

5. Module: I^2C

The BCL bit in I2CSTAT can only be cleared with Word instructions, and can be corrupted with byte instructions and bit operations.

Work around

Use Word instructions to clear BCL.

6. Module: I^2C

During I^2C communication, after a device operating in Slave mode transmits data to the master, the ACKSTAT bit in the I2CxSTAT register is set or cleared depending on whether the master sent an ACK or NACK after the byte of data. If the ACKSTAT bit is set, it will be cleared again after some delay.

Work around

Store the value of the ACKSTAT bit immediately after an I^2C interrupt occurs.

7. Module: I^2C

If there are two I^2C devices on the bus, one of them is acting as the Master receiver and the other as the Slave transmitter. If both devices are configured for 10-bit addressing mode, and have the same value in the A10 and A9 bits of their addresses, then when the Slave select address is sent from the Master, both the Master and Slave acknowledge it. When the Master sends out the read operation, both the Master and the Slave enter into Read mode and both of them transmit the data. The resultant data will be the ANDing of the two transmissions.

Work around

In all I^2C devices, the addresses as well as bits A10 and A9 should be different.

8. Module: I^2C

When the I^2C module is configured as a 10-bit slave with and address of 0x102, the I2CxRCV register content for the lower address byte is 0x01 rather than 0x02; however, the module acknowledges both address bytes.

Work around

None.

9. Module: I^2C

With the I^2C module enabled, the PORT bits and external interrupt input functions (if any) associated with the SCL and SDA pins do not reflect the actual digital logic levels on the pins.

Work around

If the SDA and/or SCL pins need to be polled, these pins should be connected to other port pins in order to be read correctly. This issue *does not* affect the operation of the I^2C module.

10. Module: I^2C

In 10-bit Addressing mode, some address matches don't set the RBF flag or load the receive register I2CxRCV, if the lower address byte matches the reserved addresses. In particular, these include all addresses with the form XX0000XXXX and XX1111XXXX, with the following exceptions:

- 001111000X
- 011111001X
- 101111010X
- 111111011X

Work around

Ensure that the lower address byte in 10-bit Addressing mode does not match any 7-bit reserved addresses.

11. Module: UART (UxE Interrupt)

The UART error interrupt may not occur, or may occur at an incorrect time, if multiple errors occur during a short period of time.

Work around

Read the error flags in the UxSTA register whenever a byte is received to verify the error status. In most cases, these bits will be correct, even if the UART error interrupt fails to occur.

12. Module: UART (IrDA)

When the UART is operating in 8-bit mode (PDSEL = 0x) and using the IrDA encoder/decoder (IREN = 1), the module incorrectly transmits a data payload of 80h as 00h.

Work around

None.

13. Module: Comparator

If CMCON<CxOUTEN> is set and the Comparator module CMCON<CxEN> is disabled, the remappable comparator output pins, C1OUT and C2OUT, cannot be used as General Purpose I/O pins.

Work around

When the Comparator module is disabled the CMCON<CxOUTEN> bit should be reset so that the remappable comparator output pins C1OUT and C2OUT are not driven onto the output pad.

14. Module: Internal Voltage Regulator

When the VREGS (RCON<8>) bit is set to a logic '0', higher sleep current may be observed.

Work around

Ensure VREGS (RCON<8>) bit is set to a logic '1' for device Sleep mode operation.

15. Module: Product Identification

Revision A2 devices marked as extended temperature range (E) devices, support only industrial temperature range (I).

Work around

Use Revision A3 devices marked as extended temperature range (E) devices.

16. Module: PSV Operations

An address error trap occurs in certain addressing modes when accessing the first four bytes of an PSV page. This only occurs when using the following addressing modes:

- MOV.D
- Register indirect addressing (word or byte mode) with pre/post-decrement

Work around

Do not perform PSV accesses to any of the first four bytes using the above addressing modes. For applications using the C language, MPLAB C30 version 3.11 or higher, provides the following command-line switch that implements a work around for the erratum.

```
-merrata=psv_trap
```

Refer to the readme.txt file in the MPLAB C30 v3.11 tool suite for further details.

17. Module: ECAN

The ECAN module may not store received data in the correct location. When this occurs, the receive buffers will become corrupted. In addition, it is also possible for the transmit buffers to become corrupted. This issue is more likely to occur as the CAN bus speed approaches 1 Mbps.

Work around

None.

18. Module: ECAN

The ECAN module does not generate a CAN event interrupt when coming out of Disable mode on bus wake-up activity even if the WAKIE bit in the CiINTE register is set. The WAKIF bit in the CiINTF register will reflect the correct status. The CAN event interrupt occurs only if the device was in Sleep mode when the bus wake-up activity occurred.

Work around

When placing the ECAN module in Disable mode, place the device in Sleep mode to be able to generate the CAN event interrupt on bus wake-up activity. If it is not possible to place the device in Sleep mode, poll the WAKIF bit in the CiINTF register to track bus wake-up activity.

APPENDIX A: REVISION HISTORY

Revision A (3/2008)

This is the initial release of this document.

Revision B (9/2008)

Added reference to silicon revisions A2 and A3. Added silicon issues 8-10 (I2C), 11 (UART (UxE Interrupt)), 12 (UART (IrDA)), 13 (Comparator), 14 (Internal Voltage Regulator), 15 (Product Identification), 16 (PSV Operations) and 17-18 (ECAN).

NOTES:

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